DOCUMENT NUMBER AND REVISION

FS-893BU01012 REV. B

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

CUSTOMER	
MODEL NUMBER	**893BU01012**
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2014.01.17	First Release.	LIANG YUN	LI HUAMING
A B	2014.08.29	1)Update the module specification.	YANG YANYAN	LI HUAMING

CONTENTS

Specification of LCD Module Type
Item No.: 893BU01012

1. General Description

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 1.54” active area contains 200×200 pixels, and has 1-bit full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM, LUT ,VCOM, and border are supplied with each panel.

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage .
- I2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 300um

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	31.8(L) × 37.32(W) × 1.18(H) (Exclude FPC) 31.8(L) × 51.42(W) × 1.18(H) (Include FPC)	mm
Active area	27.6(L) × 27.6(W)	mm
Display format	200×200	dots
Pixel Pitch	0.138(L) × 0.138(W)	mm
Pixel Configuration	Square	

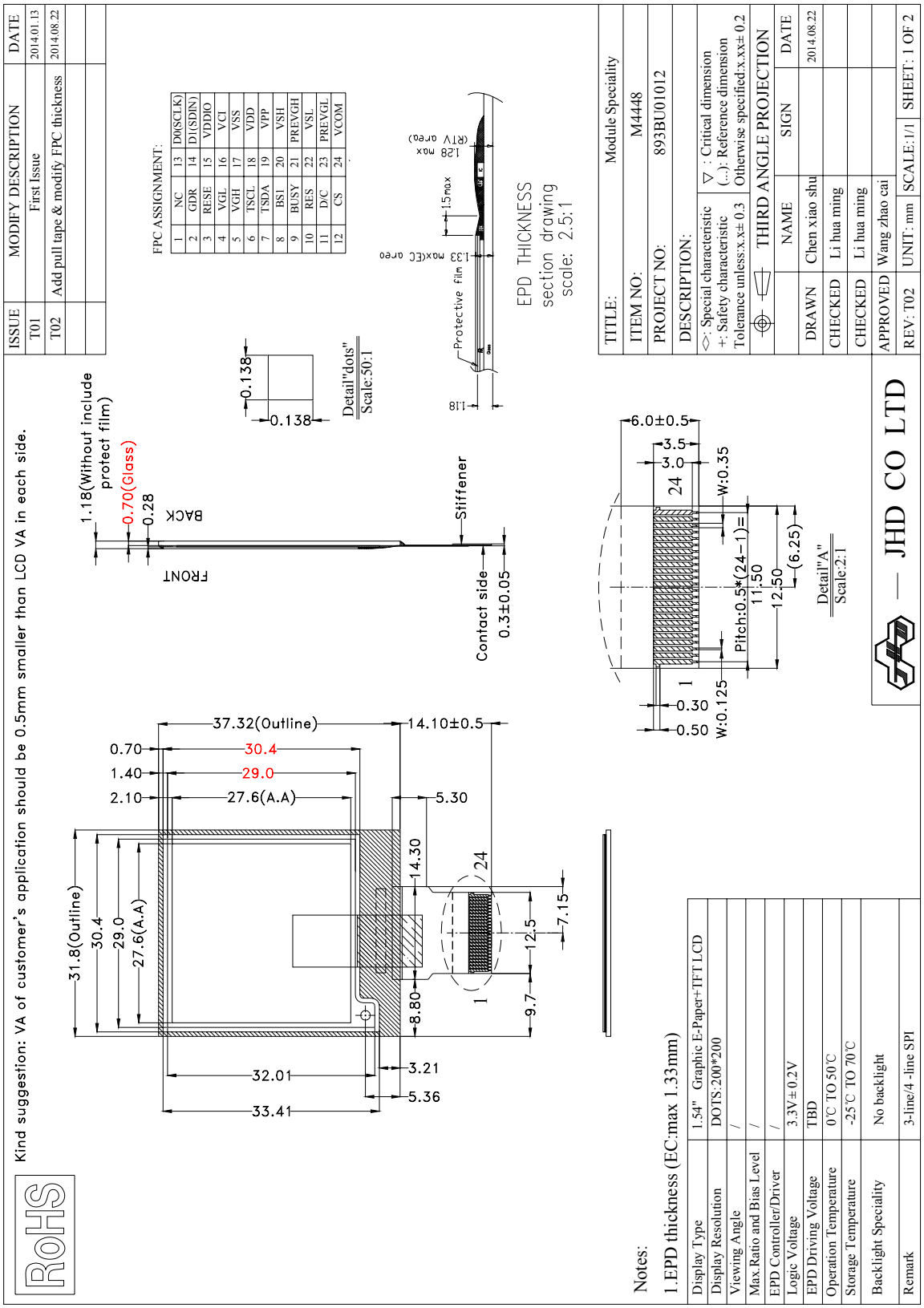


Figure 1a: Module Specification 1

ISSUE	MODIFY DESCRIPTION	DATE
T01	First Issue	2014.01.13
T02	Add pull tape & modify FPC thickness	2014.08.22

1. 晶华公司的环保标志:
   JHD Environment Sign(green shading):

RoHS

2. 晶华所执行的标准如下:
   JHD perform Environment Standard as follows :

有害物质六种含量(ppm)---ICP 测试方式 Six Injurant Contents (ppm)---ICP Test Style					
镉及镉化合物 Cadmium and Cadmium compounds	铅及铅化合物 Lead and lead compounds	汞及汞化合物 Mercury and mercury compounds	6价铬化合物 Hexavalent chromium compounds	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenylethers (PBDE)
<100	<1000	<1000	<1000	<1000	<1000

3. 如有客户环保协议,按客户环保协议执行.
   We Could Execute According To Customer's Environment Standard If Customer Requires.

— JHD CO LTD

TITLE:	Module Speciality		
ITEM NO:	M4448		
PROJECT NO:			
DESCRIPTION:			
<>: Special characteristic +: Safety characteristic Tolerance unless:x.x± 0.3	▽ : Critical dimension (...): Reference dimension Otherwise specified:x.xx± 0.2		
THIRD ANGLE PROJECTION			
	NAME	SIGN	DATE
DRAWN	Chen xiao shu		2014.08.22
CHECKED	Li hua ming		
CHECKED	Li hua ming		
APPROVED	Wang zhao cai		
REV: T02	UNIT: mm	SCALE:1/1	SHEET: 2 OF 2

Figure 1b: Module Specification 2

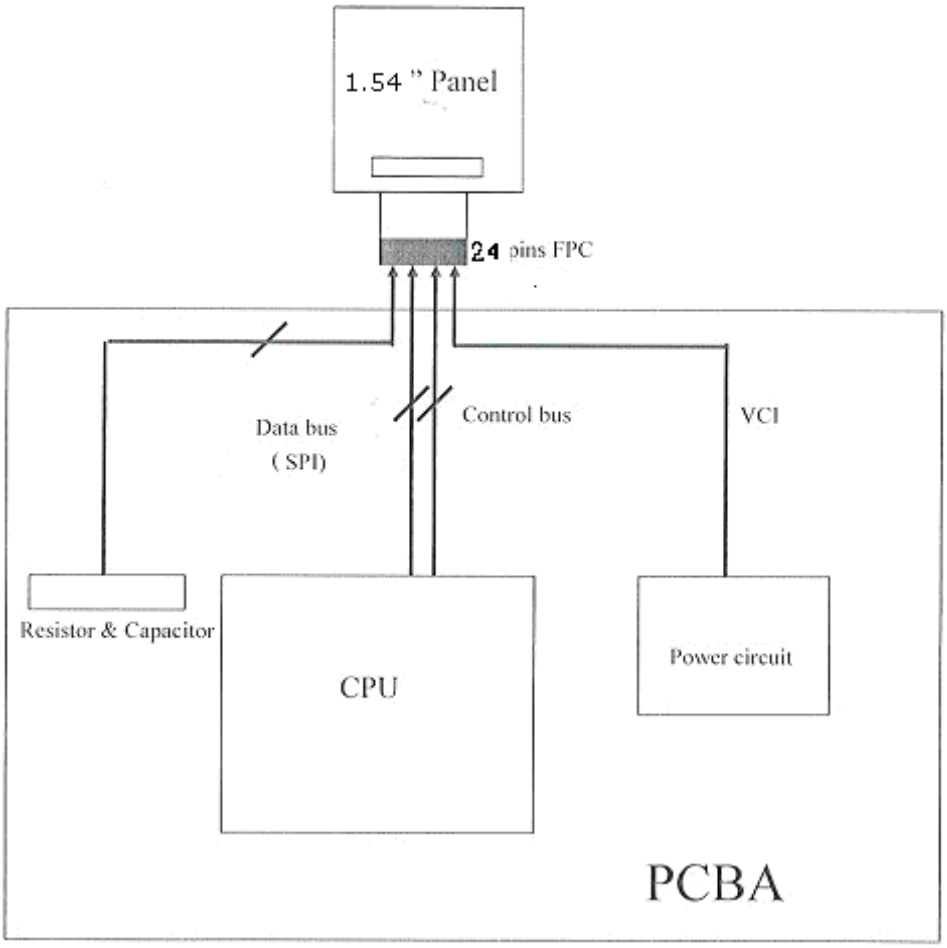


Figure 2: Block Diagram

3. Interface signals

Table 2 for FPC

Pin No.	Type	Symbol	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 5
9	O	BUSY	Busy state output pin	Note 4
10	I	RES #	Reset	Note 3
11	I	D/C #	Data /Command control pin	Note 2
12	I	CS #	Chip Select input pin	Note 1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 3: This pin (RES#) is reset signal input. The Reset is active low。

Note 4: This pin (BUSY) is Busy state output pin. When Busy is High, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put busy pin High when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected.

When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

4. Electrical Characteristics

4.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VCI	-0.5 to +3.6	V
Logic Input Voltage	VIN	-0.5 to VCI +0.5	V
Logic Output Voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp. range	TOPR	0 to +50	℃
Storage Temp. range	TSTG	-25 to +70	℃

4.2 Panel DC Characteristics

The following specifications apply for : VSS = 0V, VCI = 3.0V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	VSS	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.4	3.3	3.7	V
High level input voltage	VIH	-	0.8VCI	-	-	V
Low level input voltage	VIL	-	-	-	0.2VCI	V
High level output voltage	VOH	IOH= -100uA	0.9VCI	-	-	V
Low level output voltage	VOL	IOH= -100uA	-	-	0.1VCI	V
Image update current	IUPDATE	-	-	8	10	mA
Standby panel current	Istandby	-	-	-	5	uA
Power panel（update）	PUPDATE	-	-	26.4	-	mW
Standby power panel	PSTBY	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	40	℃
Storage temperature	-	-	-25	-	70	℃
Image updateTime at 25 ℃	-	-	-	1000	-	ms
Deep sleep mode current	VCI	DC/DC off No clock No input load Ram data not retain	-	2	5	uA
Sleep mode current	VCI	DC/DC off No clock No input load Ram data retain	-	35	50	uA

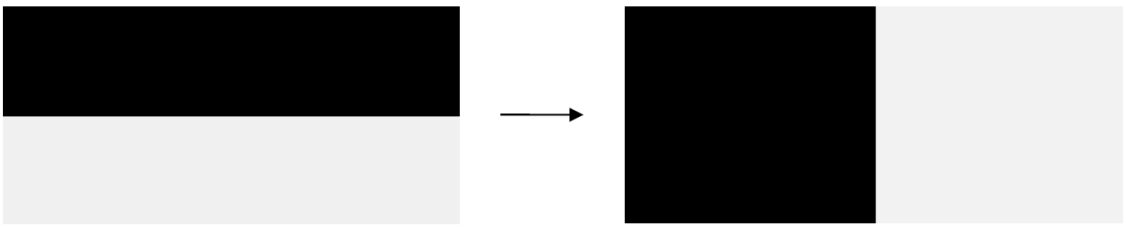
- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale

pattern to vertical 2 gray scale pattern.(Note 7-1)

- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by WF
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 1:

The Typical power consumption



4.3 Panel AC Characteristics

4.3.1 Oscillator frequency

The following specifications apply for : VSS = 0V, VCI = 3.0V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.4 to 3.7V	0.95	1	1.05	MHz

4.3.2 MCU Interface

4.3.2.1 MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Table: MCU interface assignment under different bus interface mode

Pin Name	Data /Command interface		Control signal		
Bus interface	D1	D0	CS#	D /C#	RES#
SPI4	SDin	SCLK	CS#	D /C#	RES#
SPI3	SDin	SCLK	CS#	L	RES#

Note 1: L is connected to VSS

Note 2: H is connected to VCI

4.3.2.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Table: Control pins of 4-wire Serial Peripheral interface

Function	CS#	D/C#	SCLK
Write Command	**L**	**L**	↑
Write data	**L**	**H**	↑

Note: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

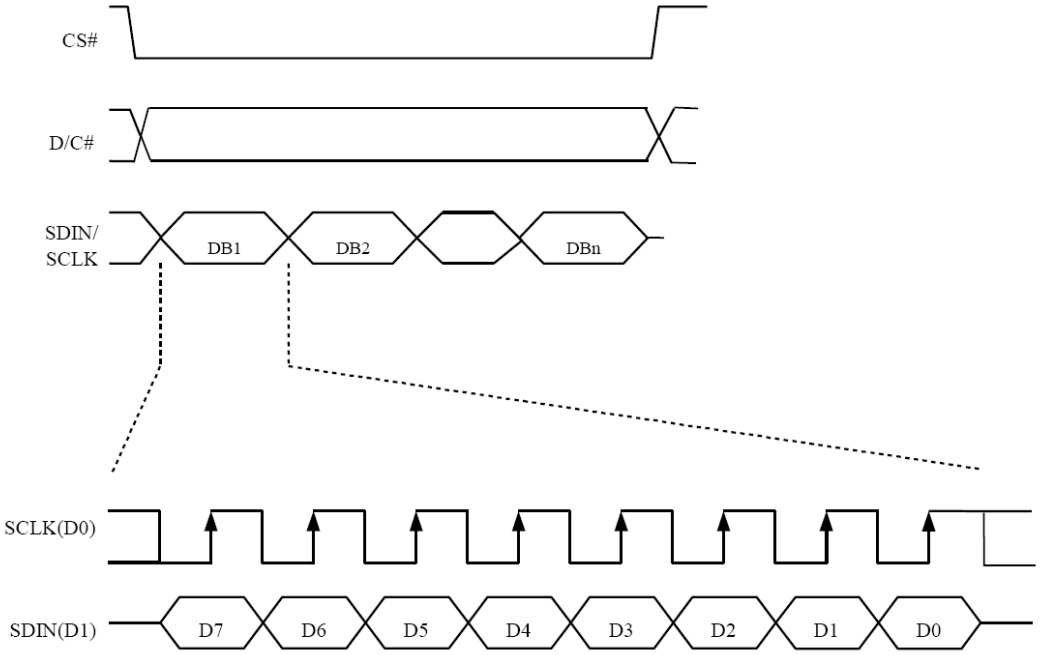


Figure : Write procedure in 4-wire Serial Peripheral Interface mode

4.3.2.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode,D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground. The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence : D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode ,only write operations are allowed.

Table: Control pins of 3-wire Serial Peripheral Interface

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Note: ↑stands for rising edge of signal

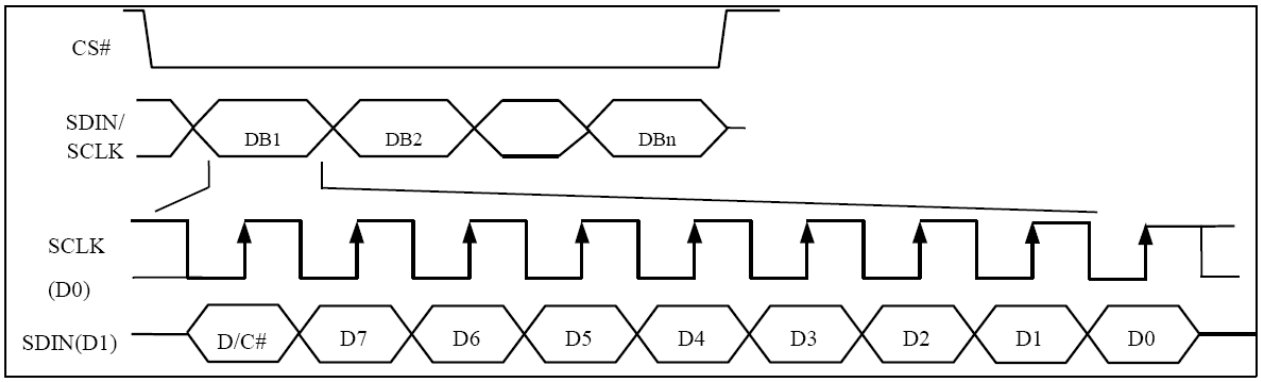


Figure: Write procedure in 3-wire Serial Peripheral Interface mode

4.3.3 Timing Characteristics of Series Interface

Table: Serial Peripheral Interface Timing Characteristics

(VCI - VSS = 1.8 V to 2.0 v , TA = 25℃, CL = 20 pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20%~80%]	-	-	15	ns
t_F	Fall Time [20%~80%]	-	-	15	ns

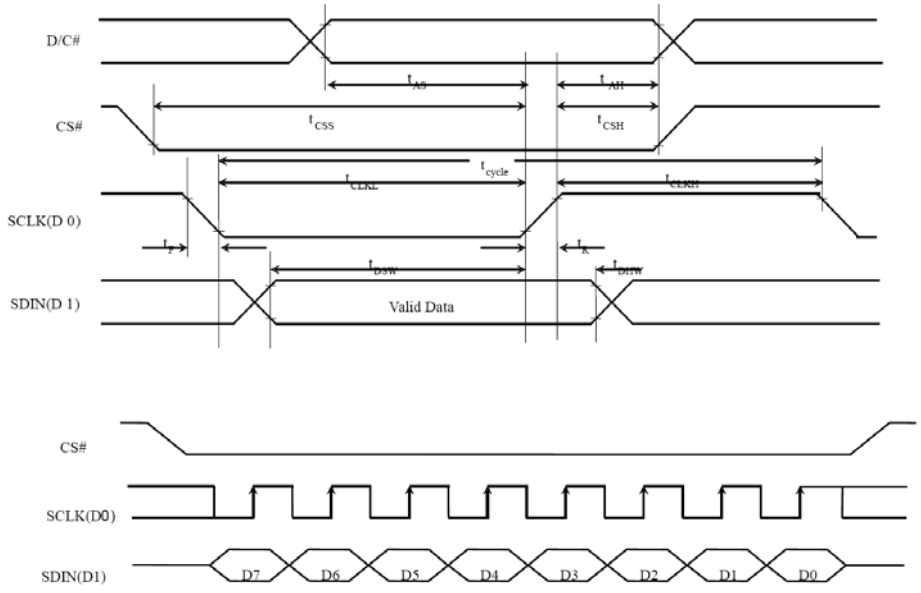
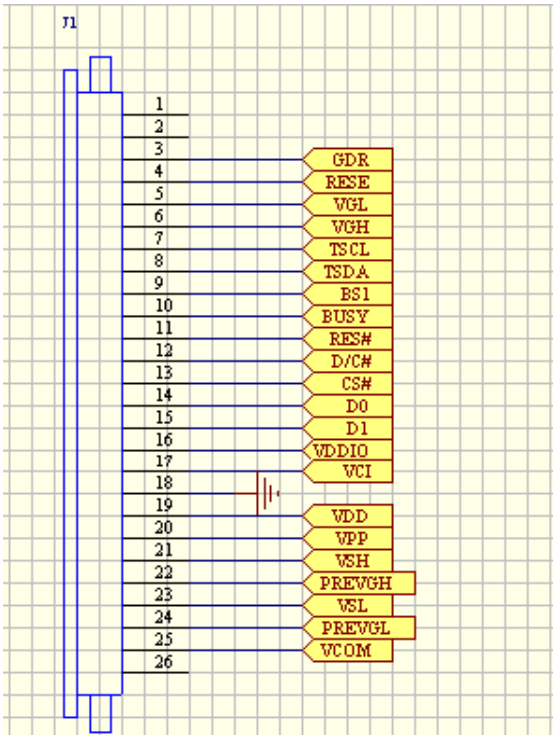


Figure: Serial peripheral interface characteristics

4.4 Power Consumption

Parameter	Symbol	Conditions	Typ.	Max.	Units	Remark
Panel power consumption during update	-	-	26.4	33	mW	-
Power consumption in standby mode	-	-	-	0.017	mW	-

4.5 Reference Circuit



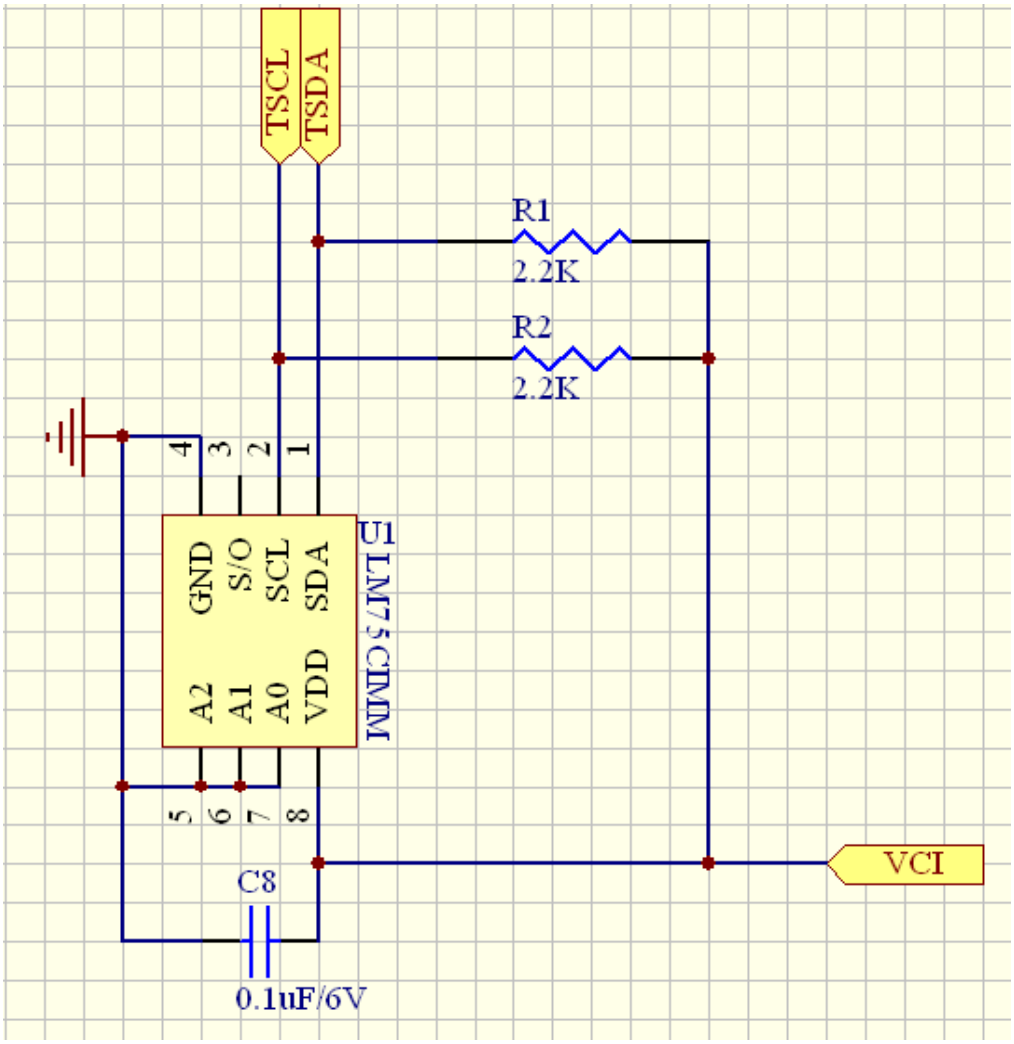

TSCL
TSDA
R1
2.2K
R2
2.2K
4
3
2
1
GND
S/O
SCL
SDA
A2
A1
A0
VDD
U1
LM75CIMM
5
6
7
8
VCI
C8
0.1uF/6V

Figure. (2)

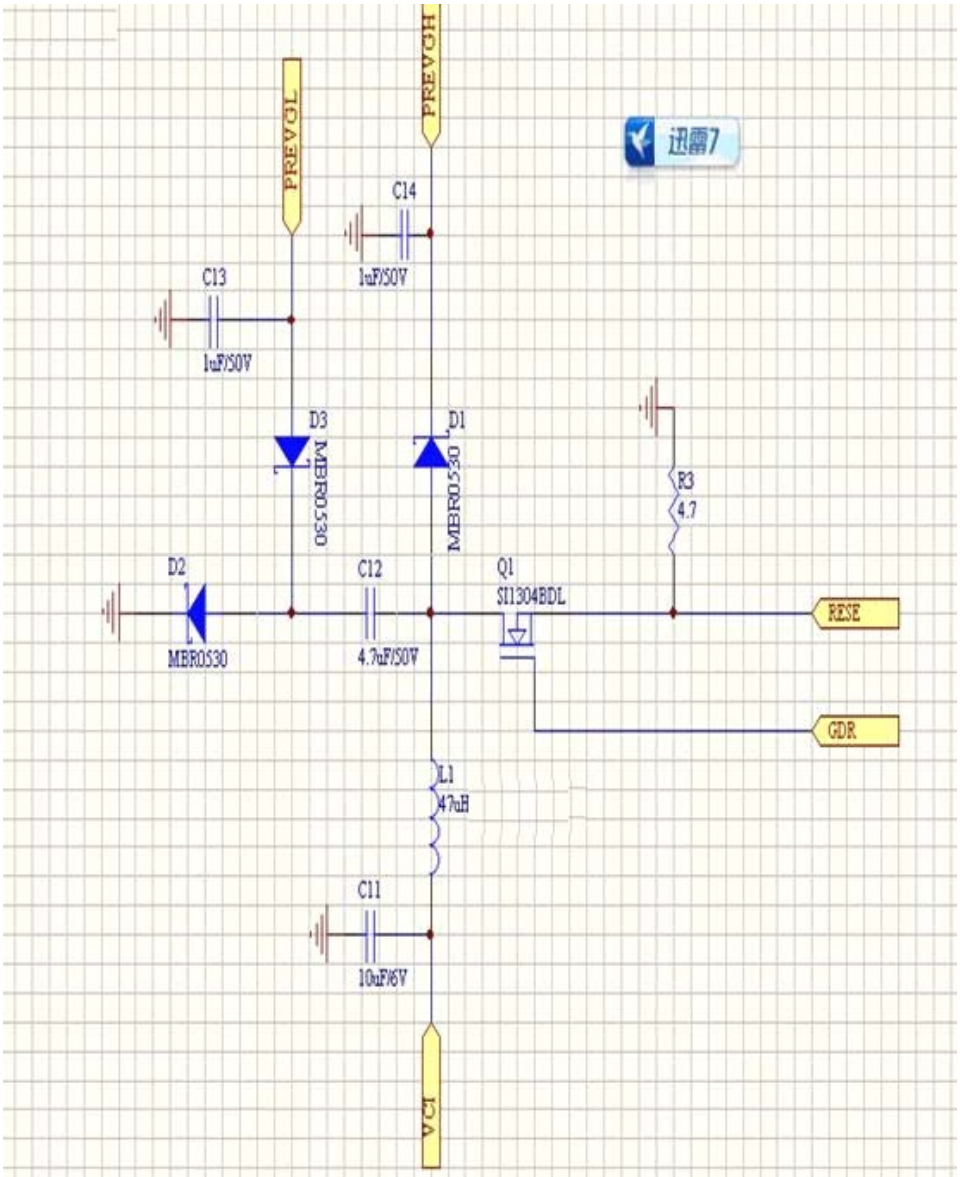
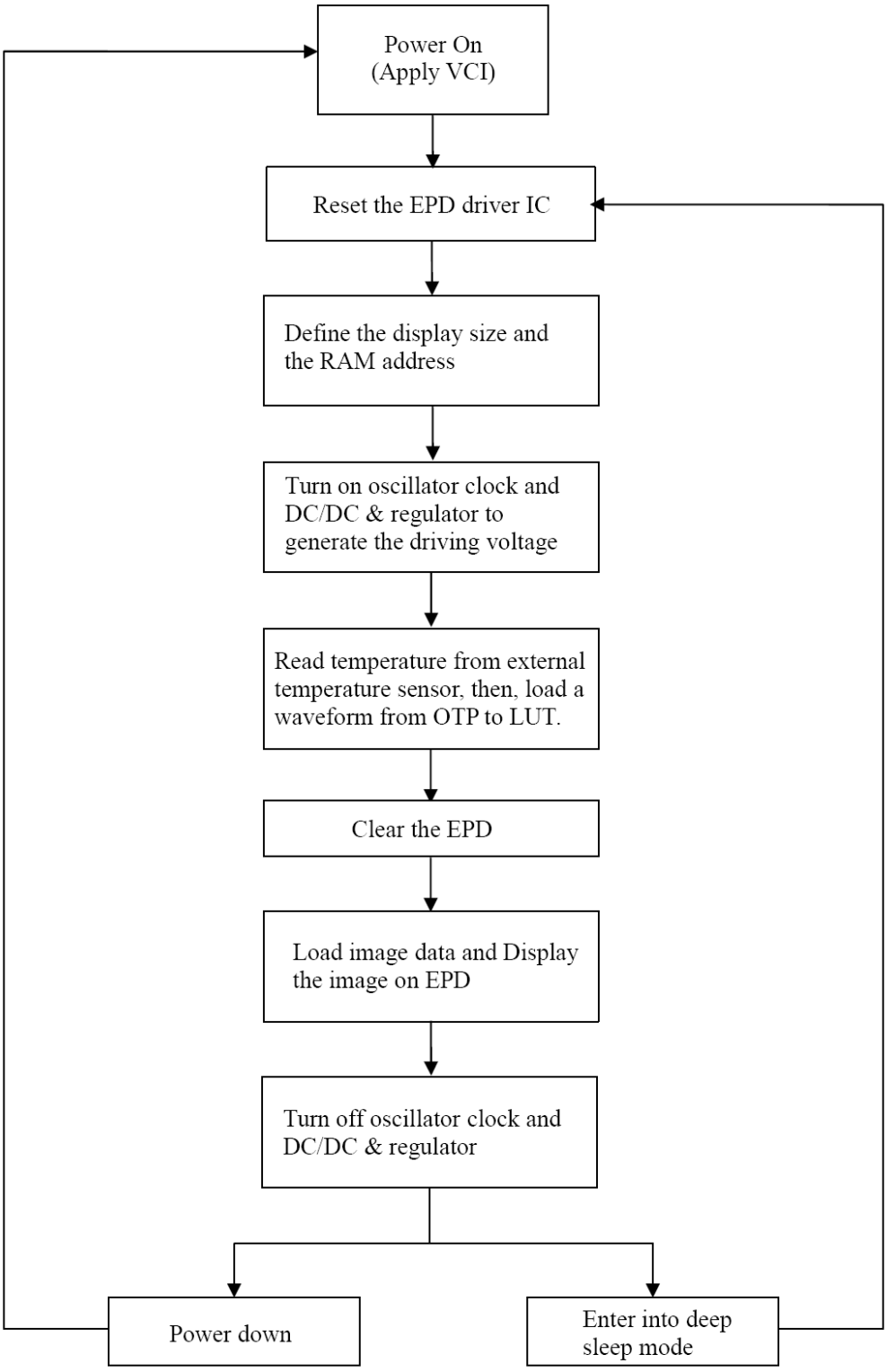


Figure. (3)

5. Typical Operating Sequence

5.1 Normal Operation Flow



6. Command Table

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]: MUX setting as A[8:0] + 1 POR = 12Bh + 1 MUX B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…G299 (left and right gate interlaced) SM=1, G0, G2, G4 …G178, G1, G3, …G299 B[0]: TB TB = 0 [POR], scan from G0 to G299 TB = 1, scan from G299 to G0.
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current setting. A[7:0] -> Soft start setting for Phase1 = 87h [POR] B[7:0] -> Soft start setting for Phase2 = 86h [POR] C[7:0] -> Soft start setting for Phase3 = 85h [POR]
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 299. When TB=0: SCN [8:0] = A[8:0] A[8:0] = 000h [POR] When TB=1: SCN [8:0] = 299 - A[8:0] A[8:0] = 000h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	1		0	0	0	0	0	0	0	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Display Update Control 1</td><td rowspan="2">Option for Display Update
Bypass Option used for Pattern Display, which is used for display the RAM content into the Display

OLD RAM Bypass option
A [7]
A[7] = 1: Enable bypass
A[7] = 0: Disable bypass [POR]

A[4] value will be used as for bypass.
A[4] = 0 [POR]

A[1:0] Initial Update Option - Source Control

<table><tr><td>A[1:0]</td><td>GSC</td><td>GSD</td></tr><tr><td>01 [POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td>Display Update Sequence Option:
Enable the stage for Master Activation

<table><tr><td></td><td>Parameter (in Hex)</td></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature value
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>FF [POR]</td></tr><tr><td>To Enable Clock Signal (CLKEN=1)</td><td>80</td></tr><tr><td>To Enable Clock Signal, then Enable CP (CLKEN=1, CPEN=1)</td><td>C0</td></tr><tr><td>To INITIAL DISPLAY + PATTEN DISPLAY</td><td>0C</td></tr><tr><td>To INITIAL DISPLAY</td><td>08</td></tr><tr><td>To DISPLAY PATTEN</td><td>04</td></tr><tr><td>To Disable CP,
then Disable Clock Signal (CLKEN=1, CPEN=1)</td><td>03</td></tr><tr><td>To Disable Clock Signal (CLKEN=1)</td><td>01</td></tr></table>Remark:
CLKEN=1:
If CLS=VDDIO then Enable OSC
If CLS=VSS then Enable External Clock
CLKEN=0:
If CLS=VDDIO then Disable OSC
AND</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
												INTERNAL CLOCK Signal = VSS,
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU [240 bits], (excluding the VSH/VSL and Dummy bit)
0 0 0 … 0 0	1 1 1 … 1 1	LUT [30 bytes]										
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0]: Number of dummy line period in term of TGate A[6:0] = 16h [POR] Available setting 0 to 127.
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE. A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD A[5:4] / VBD level: 00 / VSS; 01 / VSH; 10 / VSL; 11[POR] / HiZ A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) A[1:0] / GSA / GSB: 01 [POR] / GS0 / GS1

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], XStart, POR = 00h B[4:0]: XEA[4:0], XEnd, POR = 18h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 12Bh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD8:0], POR is 000h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

7. Optical characteristics

7.1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Min	Type	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 1
Gn	2Grey Level	-	-	DS+(WS-DS)xn(m-1)	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Tupdate	Update time		-	1	-	sec	-
Panel's life		0℃~50℃		1000000 times or 5 years			Note 2

WS: White state, DS : Dark state

Gray state from Dark to White : DS、WS

m: 2

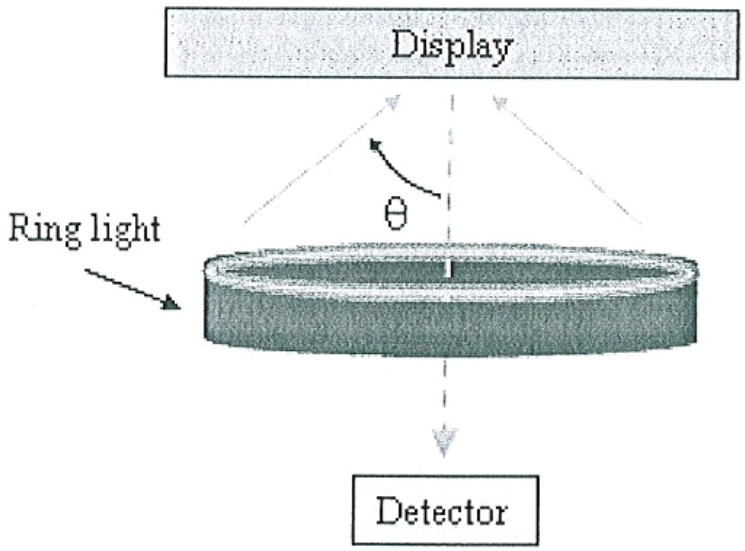
Note 1: Luminance meter : Eye – One Pro Spectrophotometer

Note 2 When work in temperature below 5 degree or above 35 degree, the panel's life will be shortened over 20%.

7.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) :

R1: white reflectance Rd: dark reflectance CR = R1/Rd

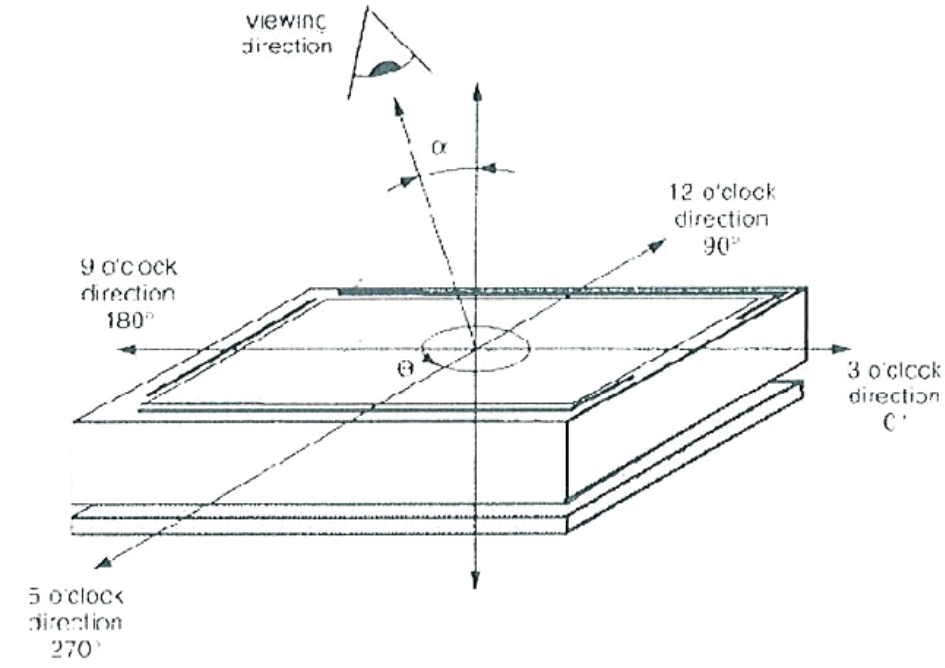


7.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor white board x (L center / L white board)

L center is the luminance measured at center in a white area (R=G =B=1) . L white board is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees .



7.4 Bi-stability

1. 1 Month defined as no more than 20% drop of Contrast ratio.(And a general impression that the display still nice.)

Bi-stability	Result
250 hours	CR >8
500 hours	CR >8
750 hours	CR >7.5
1000 hours	CR >7

8. Reliability test

	Test	Condition	Method	Remark
1	High-Temperature Operation	T = 50℃,30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70℃, 23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=+40℃,RH=90%for168hrs	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=+60℃,RH=80%for240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	[-25℃ 30mins]→ [+70℃ 30mins] ,70cycles Test in white pattern	IEC 60 068-2-14NB	
8	UV exposure Resistance	765 W/m2 for 168 hrs,40℃	IEC 60 068-2-5 Sa	
9	Electrostatic Effect (non-operating)	Machine mode +/- 250V, 0Ω,200pF	IEC62179, IEC62180	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
12	Altitude test Operation	700hPa (=3000 m),48Hr		
13	Altitude test Storage	260hPa (=10000 m),48Hr Test in white pattern		
14	Stylus Tapping	POLYACETAL Pen: Top R:0.8mm Load: 300gf Speed: 30times/min Total 13,500times,	Test should be done with a bezel	Pass criteria – no glass breakage ordamage tomicrocapsules

Actual EMC level to be measured on customer application.

Note: The protective film must be removed before temperature test.

9. Handling， Safety And Enviromental Requirements

Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution
The display module should not be exposed to harmful gases , such as acid and alkali gases , which corrode electronic components.

Observe general precautions that are common to handling delicate electronic components . The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied . Exposure to limiting values for extended periods may affect device reliability.	
Application Information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
ROHS

10. Point and line standard

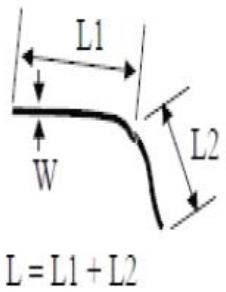
Shipment Inseption Standard

Equipment：Electrical test fixture, Point gauge

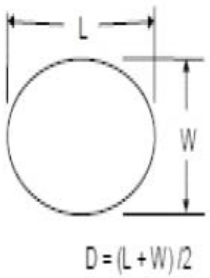
Outline demension：

29.2(H)*59.2(V)*1.18(D)

Environment	Temperature	Humidity	Illumination	Distance	Time	Angle
	20℃～25℃	40%～55%RH	800～1200Lux	200～300 mm	35Sec	rolate30° surround
appearence standard	Defet type	Inspection	Standard		Part-A	
	1. dead/ switch point (point overproof)	Electric Display	D≤0.25 mm		Ignore	
			0.25 mm < D≤0.4 mm		N≤4	
			D > 0.4 mm		Not Allow	
	2. Line (No switch)	L ＜ 0.24, W ＜0.06	- -	Ignore	No defect within 20mm range of PartA	
		0.24≤L≤ 0.4; 0.06≤W≤ 0.1	- -	4		
		L>0.4; W> 0.1	- -	0	Part-A	
	3. line (Switching line)	Electric Display	Ignore in gray scale viewing In Blak&white viewing Follow Non-Switching Criteria			
	3. Display unwork	Electric Display	Not Allow			
	4. Display error	Electric Display	Not Allow			
	5. PS PET warping	Vsual	cannot beyond 1/2 of the border			
	6. Protector hurt	Vsual	L≤2 mm, W≤0.05 mm, Ignore;			
			L>2 mm, W>0.05 mm, Not Allow;			
	7. Drawing tape	Vsual	Drawing NO. WFQC-011			
	8. Barcode label	Vsual	Drawing NO. WFQC-012			
	9. Adhesive coating	Vsual	Bubble:D≤0.65 & N≤2			
	10. Packing	Vsual	cannot be dirty and breakdown;must be marked and identified			
Remark	1. Cannot be defect&failure cause by appearence defect;					
	2. Cannot be larger size cause by appearence defect;					



Line Defect



Spot Defect

L=long W=wide D=point size

"Shenzhen Jinghua Displays CO., LTD. reserves the right to change this specification"

- END -

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