



SPECIFICATIONS FOR OLED MODULE

CUSTOMER	
MODEL	WH1602AYITF003 VER.00
CUSTOMER APPROVED	

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Module Classification Information

W H 1602 A Y I T F 003

① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

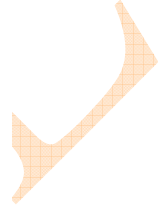
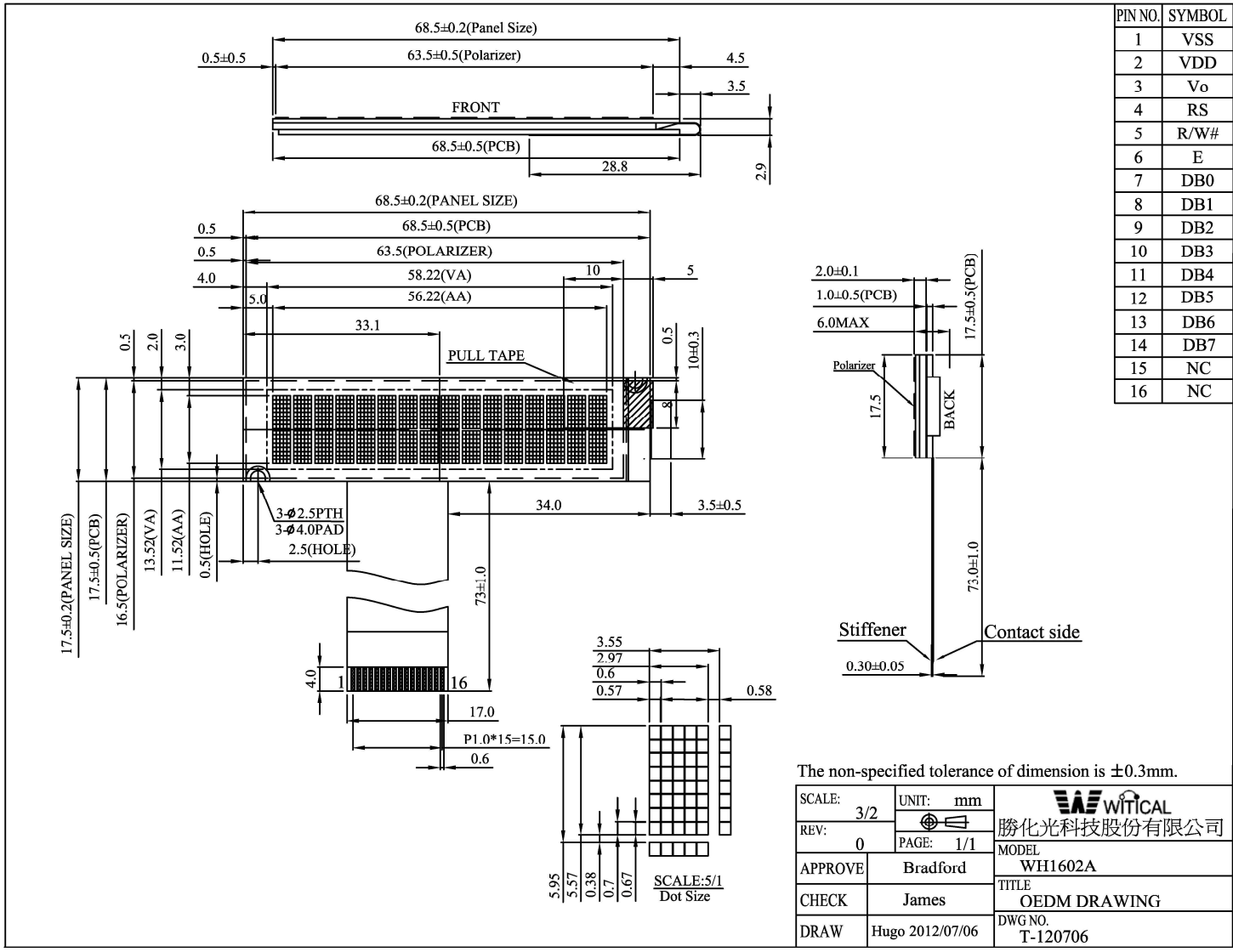
1	Brand : WITICAL CORPORATION		
2	Display Type : H→ Character Type ; G→ Graphic Type		
3	Displays Logical Dimensions : 16 x 2 Characters		
4	Serials code		
5	Emitting Color	B : Blue	R : Red
		G : Green	C : Full color
		Y : Yellow	W : White
6	Polarizer	I : With Polarizer ; O : Without Polarizer	
7	Driver Voltage	T : 3.0 V ; F : 5.0V	
8	Touch Panel	T : With touch panel ; F : Without touch panel	
9	Serial No.	000 : 6800 interface 001 : 8080 interface 002 : SPI interface 003 : I2C interface Other : Sales code	

History of Version

Version	Contents	Date	Note
00	NEW VERSION	2013/02/23	Spec.

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(1)Dimension



(2) ABSOLUTE MAXIMUM RATING

2.1 Electrical Absolute Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply for Logic	V _{DD}	-0.3	3.0	3.6	Volt	1,2
Input Voltage for I/O Pins	V _I	-0.3	3.0	3.6	Volt	1,2
Life Time (100 cd/m ²)		---	200,000	---	Hour	3

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.

Note 3: T_a = 25°C, 25% Checkerboard.

Software configuration follows Section ACTUAL APPLICATION EXAMPLE Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

2.2 Environmental Absolute Maximum Ratings

Item	Wide Temperature			
	Operating		Storage	
	Min.	Max.	Min.	Max.
Ambient Temperature	-40°C	+85°C	-40°C	+85°C

(3) ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ	Max.	Unit
Power Supply for Logic	V_{DD}	(Wide Voltage I/O Application)	2.8	3.0	3.3	Volt
Input Voltage for I/O Pins	V_i		2.8	3.0	3.3	Volt
Input Voltage	V_{IL}	L level	0	-	$0.2 V_{DD}$	Volt
	V_{IH}	H level	$0.8 V_{DD}$	-	V_{DD}	Volt
Output Voltage	V_{OL}	L level	0	-	$0.1 V_{DD}$	
	V_{OH}	H level	$0.9 V_{DD}$	-	V_{DD}	
Power Supply Current for OLED	I_{DD}	Note	-	20		mA
Sleep Mode Current for V_{DD}	$I_{DD,SLEEP}$			2	10	μA

Note : $V_{DD} = 3.0V$, 25% Display Area Turn on. 100 cd/m^2
 When random texts pattern is running , averagely , about 1/4 of pixels will be on.

(4) OPTICAL CHARACTERISTICS

Item	Symbol	Min.	Typ	Max.	Unit
Viewing angle range			Free		Degree
Dark Room Contrast	Cr		>10,000:1		
Brightness	Lbr		120		cd/m^2
Peak Emission Wavelength	C.I.E 1931 (Yellow)	X=0.46 Y=0.45	X=0.50 Y=0.49	X=0.54 Y=0.53	

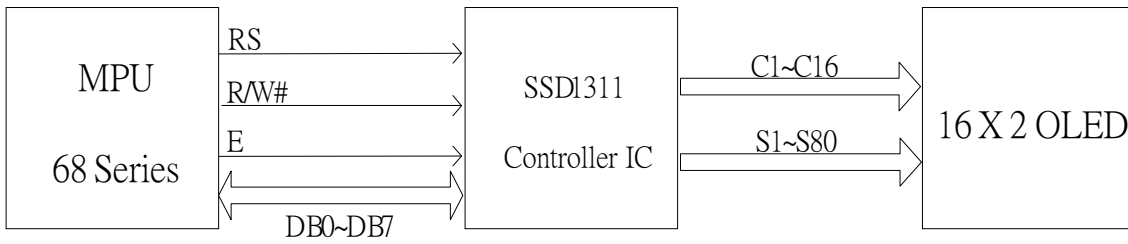
(5)MECHANICAL SPECIFICATION

Item	Description
Product No.	WH1602AYITF003
Active Area	56.22(W)mm×11.52(H)mm
Viewing Area	58.22(W)mm×13.52(H)mm
Module Size	68.5W)×17.5(H)×6 max(D)
Dot Size	0.57(W)mm×0.67(H)mm
Dot Pitch	0.60(W)mm×0.70(H)mm
Display Format	16 characters (W)×2 lines (H)
Duty Ratio	1/16 Duty
Controller	SSD1311 or Equivalent

(6)INTERFACE PIN ASSIGNMENT

Pin No.	Symbol	External Connection	Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic
3	Vo	—	Contrast Adjustment
4	RS(D/C#)	MPU	Register select signal. H: DATA, L: Command
5	NC	—	No Connect
6	NC	—	No Connect
7-14	DB0-DB7	MPU	8- bit Bi- directional data bus lines I2C- interface: DB0 will be the Bus Clock signal SCL ; DB1 will be the Bus data input SDA and Bus data output SDA .
15	NC	—	No Connect
16	NC	—	No Connect

(7) BLOCK DIAGRAM

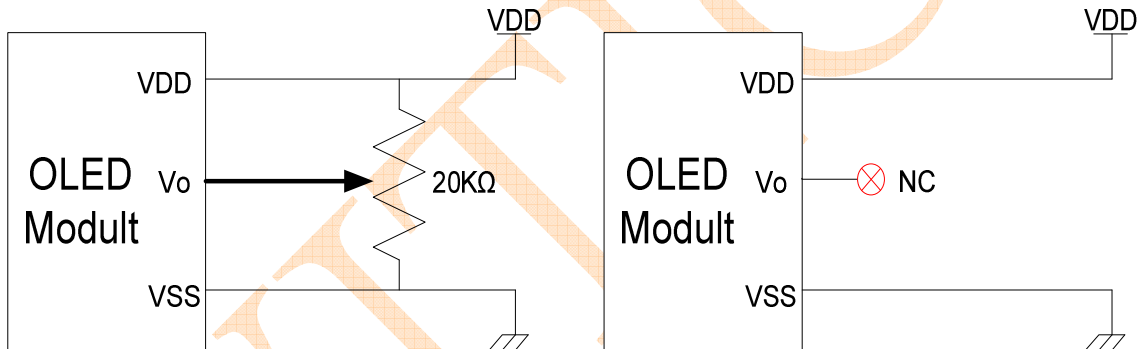


Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
DD RAM Address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

(8) POWER SUPPLY

HW&SW Contrast Adjustable

SW Contrast Adjustable



(9)FUNCTIONAL SPECIFICATION

COMMAND TABLE

There are three sets of command set in SSD1311: Fundamental Command Set, Extended Command Set and OLED Command Set. These three command sets can be selected by setting logic bits IS, RE and SD accordingly.

Table 9-1: Fundamental Command Table

1. Fundamental Command Set															
Command	IS	RE	SD	Instruction Code										Description	
				D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0		
Clear Display	X	X	0	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	X	0	0	0	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	X	0	0	0	0	0	0	0	0	0	1	I/D	S		Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	X	1	0	0	0	0	0	0	0	0	1	BDC	BDS		Common bi-direction function. BDC = "0": COM31 -> COM0 BDC = "1": COM0 -> COM31 Segment bi-direction function. BDS = "0": SEG99 -> SEG0, BDS = "1": SEG0 -> SEG99
Display ON / OFF Control	X	0	0	0	0	0	0	0	0	1	D	C	B		Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR). Note: It is recommended to turn off the cursor and blinking effects when updating internal RAM contents for better visual performance;

1. Fundamental Command Set

Command	IS	RE	SD	Instruction Code										Description	
				D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0		
Extended Function Set	X	1	0	0	0	0	0	0	0	0	1	FW	B/W	NW	<p>Assign font width, black/white inverting of cursor, and 4-line display mode control bit.</p> <p>FW = "1": 6-dot font width, FW = "0": 5-dot font width (POR),</p> <p>B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable (POR)</p> <p>NW = "1": 3-line or 4-line display mode (POR) NW = "0": 1-line or 2-line display mode</p>
Cursor or Display Shift	0	0	0	0	0	0	0	0	0	1	S/C	R/L	*	*	<p>Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.</p> <p>S/C = "1": display shift, S/C = "0": cursor shift,</p> <p>R/L = "1": shift to right, R/L = "0": shift to left</p>
Double Height (4- line) / Display-dot shift	0	1	0	0	0	0	0	0	0	1	UD2	UD1	*	DH'	<p>UD2~1: Assign different double height format (POR=11b)</p> <p>DH' = "1": display shift enable DH' = "0": dot scroll enable (POR)</p>
Shift Enable	1	1	0	0	0	0	0	0	0	1	DS4	DS3	DS2	DS1	<p>DS[4:1]=1111b (POR) when DH' = 1b</p> <p>Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.</p>
Scroll Enable	1	1	0	0	0	0	0	0	0	1	HS4	HS3	HS2	HS1	<p>HS[4:1]=1111b (POR) when DH' = 0b</p> <p>Determine the line for horizontal smooth scroll.</p> <p>HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.</p>

1. Fundamental Command Set

Command	IS	RE	SD	Instruction Code										Description
				D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	
Function Set	X	0	0	0	0	0	0	1	*	N	DH	RE (0)	IS	Numbers of display line, N when N = "1" (POR): 2-line (NW=0b) / 4-line (NW=1b), when N = "0": 1-line (NW=0b) / 3-line (NW=1b) DH = "1/0": Double height font control for 2-line mode enable/ disable (POR=0) Extension register, RE ("0") Extension register, IS
	X	1	0	0	0	0	0	1	*	N	BE	RE (1)	REV	CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Extension register, RE ("1") Reverse bit REV = "1": reverse display, REV = "0": normal display (POR)
Set CGRAM address	0	0	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. (POR=00 0000)
Set DDRAM Address	X	0	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. (POR=000 0000)
Set Scroll Quantity	X	1	0	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll. (POR=00 0000) Valid up to SQ[5:0] = 110000b
Read Busy Flag and Address/ Part ID	X	X	0	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
Write data	X	X	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM).
Read data	X	X	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM).

Table 9-2: Extended Command Table

2. Extended Command Set																																								
Command	IS	RE	SD	Instruction Code											Description																									
				D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0																										
Function Selection A	X	1	0	0	0	71	0	1	1	1	0	0	0	1	A[7:0] = 00h, Disable internal V _{DD} regulator at 5V I/O application mode A[7:0] = 5Ch, Enable internal V _{DD} regulator at 5V I/O application mode (POR)																									
	X	1	0	1	0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																										
Function Selection B	X	1	0	0	0	72	0	1	1	1	0	0	1	0	<p>OP[1:0]: Select the character no. of character generator</p> <table border="1"> <thead> <tr> <th>OP[1:0]</th> <th>CGROM</th> <th>CGRAM</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>240</td> <td>8</td> </tr> <tr> <td>01b</td> <td>248</td> <td>8</td> </tr> <tr> <td>10b</td> <td>250</td> <td>6</td> </tr> <tr> <td>11b</td> <td>256</td> <td>0</td> </tr> </tbody> </table> <p>RO[1:0]: Select character ROM</p> <table border="1"> <thead> <tr> <th>RO[1:0]</th> <th>ROM</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>A</td> </tr> <tr> <td>01b</td> <td>B</td> </tr> <tr> <td>10b</td> <td>C</td> </tr> <tr> <td>11b</td> <td>Invalid</td> </tr> </tbody> </table> <p>Note: It is recommended to turn off the display (cmd 08h) before setting no. of CGRAM and defining character ROM, while clear display (cmd 01h) is recommended to sent afterwards</p>	OP[1:0]	CGROM	CGRAM	00b	240	8	01b	248	8	10b	250	6	11b	256	0	RO[1:0]	ROM	00b	A	01b	B	10b	C	11b	Invalid
	OP[1:0]	CGROM	CGRAM																																					
00b	240	8																																						
01b	248	8																																						
10b	250	6																																						
11b	256	0																																						
RO[1:0]	ROM																																							
00b	A																																							
01b	B																																							
10b	C																																							
11b	Invalid																																							
X	1	0	1	0	0	*	*	*	*	RO1	RO0	OP1	OP0																											
OLED Characterization	X	1	X	0	0	78 / 79	0	1	1	1	1	0	0	SD	<p>Extension register, SD SD = 0b: OLED command set is disabled (POR) SD = 1b: OLED command set is enabled Details refer to Table 9-3.</p>																									
	X	1	X																																					

Notes

- (1) POR stands for Power On Reset Values.
- (2) "*" and "X" stand for "Don't care".

Table 9-3: OLED Command Table

3. OLED Command Set																																	
Command	IS	RE	SD	Instruction Code											Description																		
				D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0																			
Set Contrast Control	X	1	1	0	0	81	1	0	0	0	0	0	0	0	1	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 7Fh)																	
	X	1	1	0	0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																			
Set Display Clock Divide Ratio/Oscillator Frequency	X	1	1	0	0	D5	1	1	0	1	0	1	0	1	A[3:0] : Define the divide ratio (D)of the display clocks (DCLK): Divide ratio= A[3:0] + 1 (POR=0000b) A[7:4] : Set the Oscillator Frequency, F _{OSC} . Oscillator Frequency increases with the value of A[7:4] and vice versa. (POR=0111b) Range:0000b~1111b Frequency increases as setting value ncreases.																		
	X	1	1	0	0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																			
Set Phase Length	X	1	1	0	0	D9	1	1	0	1	1	0	0	1	A[3:0] : Phase 1 period of up to 32 DCLK; clock 0 is an valid entry with 2 DCLK (POR=1000b) A[7:4] : Phase 2 period of up to 15 DCLK; clock 0 is invalid entry (POR=0111b)																		
	X	1	1	0	0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																			
Set SEG Pins Hardware Configuration	X	1	1	0	0	DA	1	1	0	1	1	0	1	0	A[4]=0b, Sequential SEG pin configuration A[4]=1b (POR), Alternative (odd/even) SEG pin configuration A[5]=0b (POR), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap																		
	X	1	1	0	0	A[5:4]	0	0	A ₅	A ₄	0	0	0	0																			
Set VCOMH Deselect Level	X	1	1	0	0	DB	1	1	0	1	1	0	1	1	<table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Hex code</th> <th>V_{COMH} deselect level</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>00h</td> <td>~ 0.65 x VCC</td> </tr> <tr> <td>000b</td> <td>10h</td> <td>~ 0.71 x VCC</td> </tr> <tr> <td>010b</td> <td>20h</td> <td>~ 0.77 x VCC (POR)</td> </tr> <tr> <td>011b</td> <td>30h</td> <td>~ 0.83 x VCC</td> </tr> <tr> <td>100b</td> <td>40h</td> <td>1 x VCC</td> </tr> </tbody> </table>	A[6:4]	Hex code	V _{COMH} deselect level	000b	00h	~ 0.65 x VCC	000b	10h	~ 0.71 x VCC	010b	20h	~ 0.77 x VCC (POR)	011b	30h	~ 0.83 x VCC	100b	40h	1 x VCC
A[6:4]	Hex code	V _{COMH} deselect level																															
000b	00h	~ 0.65 x VCC																															
000b	10h	~ 0.71 x VCC																															
010b	20h	~ 0.77 x VCC (POR)																															
011b	30h	~ 0.83 x VCC																															
100b	40h	1 x VCC																															
	X	1	1	0	0	A[6:4]	0	A ₆	A ₅	A ₄	0	0	0	0																			

3. OLED Command Set

Command	IS	RE	SD	Instruction Code											Description														
				D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0															
Function Selection C	X X	1 1	1 1	0 0	0 0	DC A[7:0]	1 A ₇	1 0	0 0	1 0	1 0	1 0	0 A ₁	0 A ₀	<p>Set VSL & GPIO</p> <p>Set VSL: A[7] = 0b: Internal VSL (POR) A[7] = 1b: Enable external VSL</p> <p>Set GPIO: A[1:0] = 00b represents GPIO pin HiZ, input disabled (always read as low) A[1:0] = 01b represents GPIO pin HiZ, input enabled A[1:0] = 10b represents GPIO pin output Low (RESET) A[1:0] = 11b represents GPIO pin output High</p>														
Set Fade Out and Fade in / out	X X	1 1	1 1	0 0	0 0	23 A[5:0]	0 *	0 *	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	<p>A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET]</p> <p>A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled.</p> <p>A[5:4] = 11b Enable Fade in / out mode. Once Fade in / out mode is enabled, contrast decrease gradually to all pixels OFF and then contrast increase gradually to normal display. This process loop continuously until the Fade in / out mode is disabled.</p> <p>A[3:0] : Set time interval for each fade step</p> <table border="1"> <thead> <tr> <th>A[3:0]</th> <th>Time interval for each fade step</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>8 Frames</td> </tr> <tr> <td>0001b</td> <td>16 Frames</td> </tr> <tr> <td>0010b</td> <td>24 Frames</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>1110b</td> <td>120 Frames</td> </tr> <tr> <td>1111b</td> <td>128 Frames</td> </tr> </tbody> </table>	A[3:0]	Time interval for each fade step	0000b	8 Frames	0001b	16 Frames	0010b	24 Frames	:	:	1110b	120 Frames	1111b	128 Frames
A[3:0]	Time interval for each fade step																												
0000b	8 Frames																												
0001b	16 Frames																												
0010b	24 Frames																												
:	:																												
1110b	120 Frames																												
1111b	128 Frames																												

Note

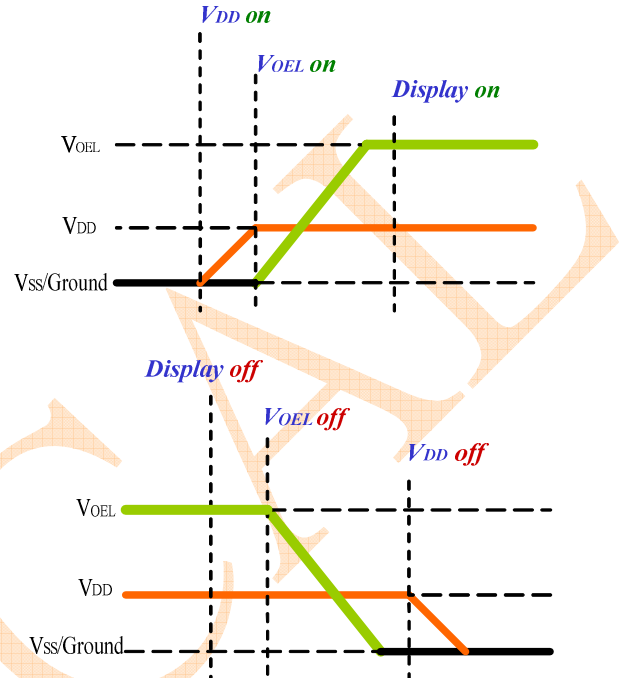
- (1) POR stands for Power On Reset Values.
- (2) "*" and "X" stand for "Don't care".
- (3) The locked OLED driver IC MCU interface prohibits all commands access except logic bit SD is set to 1b.
- (4) Refer to Table 9-1 and Table 9-2 for the details of logic bits IS, RE and SD.

(10) Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{OEL}
6. Delay 100ms
(When V_{OEL} is stable)
7. Send Display on command



Power down Sequence:

1. Send Display off command
2. Power down V_{OEL}
3. Delay 100ms
(When V_{OEL} is reach 0 and panel is completely discharges)
4. Power down V_{DD}

Note:

- 1) Since an ESD protection circuit is connected between V_{DD} and V_{OEL} inside the driver IC, V_{OLE} becomes lower than V_{DD} whenever V_{DD} is ON and V_{OEL} is OFF.
- 2) V_{OEL} should be kept float (disable) when it is OFF.
- 3) Power Pins (V_{DD} , V_{OEL}) can never be pulled to ground under any circumstance.
- 4) V_{DD} should not be power down before V_{OEL} power down.

Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 5X8 Character Mode
3. Display start position is set at display RAM address 0
4. CGRAM address counter is set at 0
5. Cursor is OFF
6. Blink is OFF
7. Contrast control register is set at 7Fh
8. OLED command set is disabled

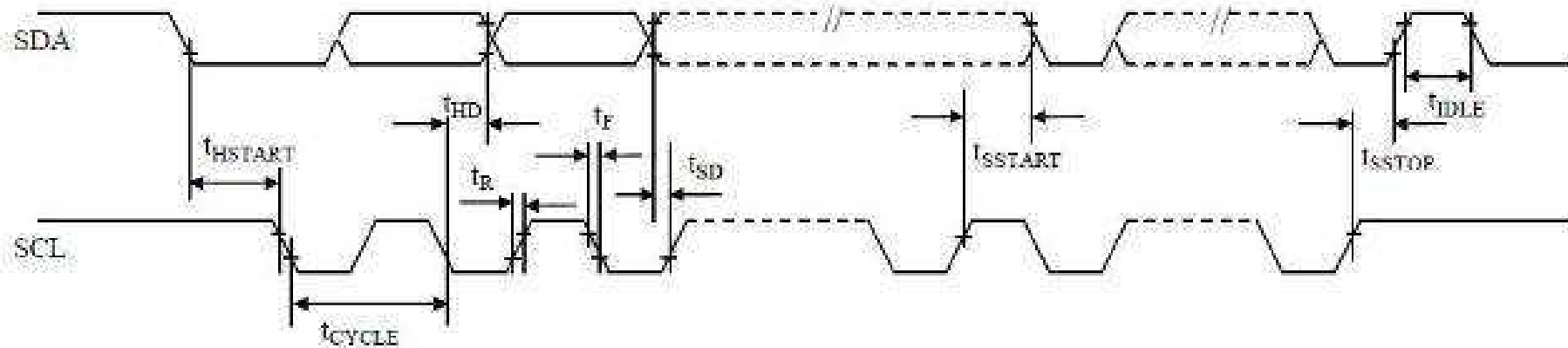
(11) MCU I2C Interface Timing Characteristics

(TA = 25°C , VDD = 4.5~5.5V, VSS =0V)

Symbol	Description	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time	2.5	-	-	us
t _{HSTART}	Start Condition Hold Time	0.6	-	-	us
t _{HD}	Data Hold Time (for "SDA _{OUT} " pin)	5	-	-	ns
	Data Hold Time (for "SDA _{IN} " pin)	460	-	-	ns
t _{SD}	Data Setup Time	100	-	-	ns
t _{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t _{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t _R	Rise Time for data and clock pin	-	-	300	ns
t _F	Fall Time for data and clock pin	-	-	300	ns
t _{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

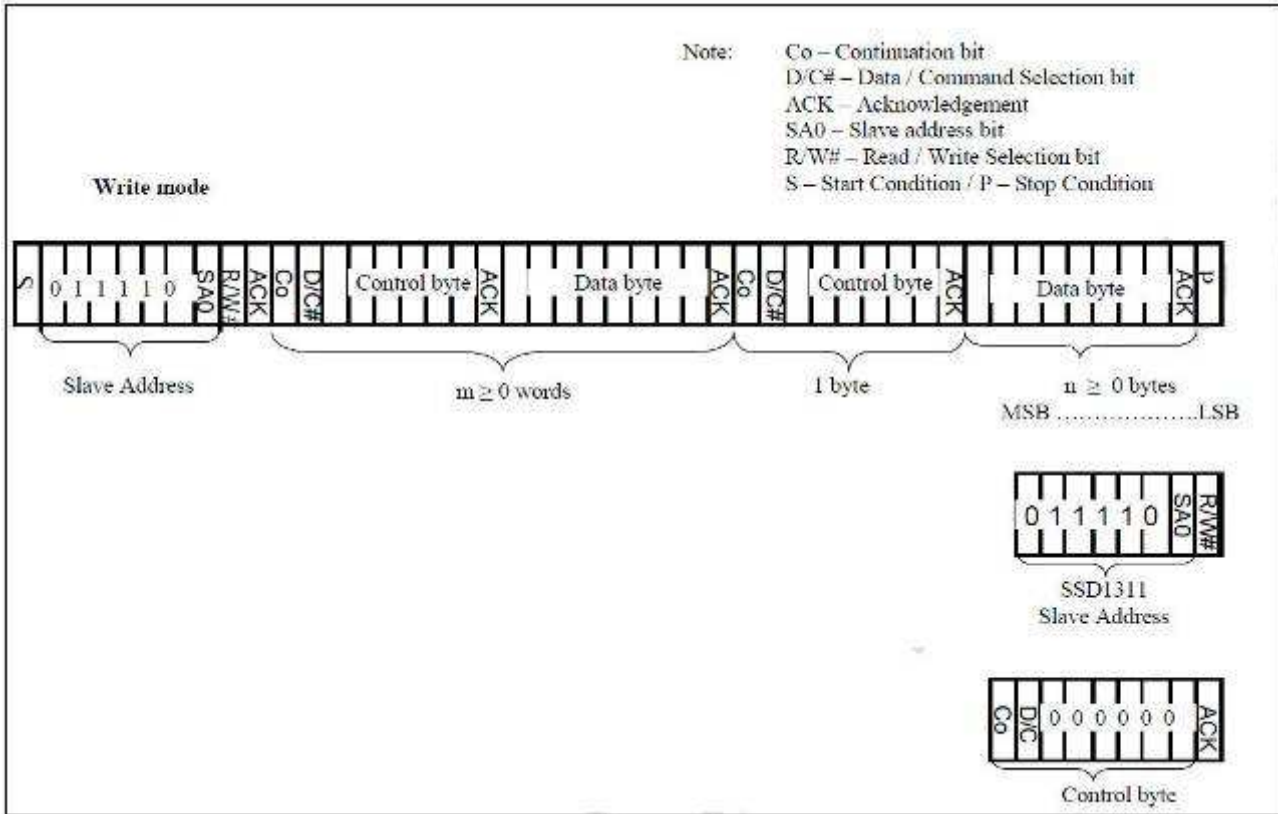
Note : I2C Timing Characteristics

All timings are based on 20% to 80% of VDD-V



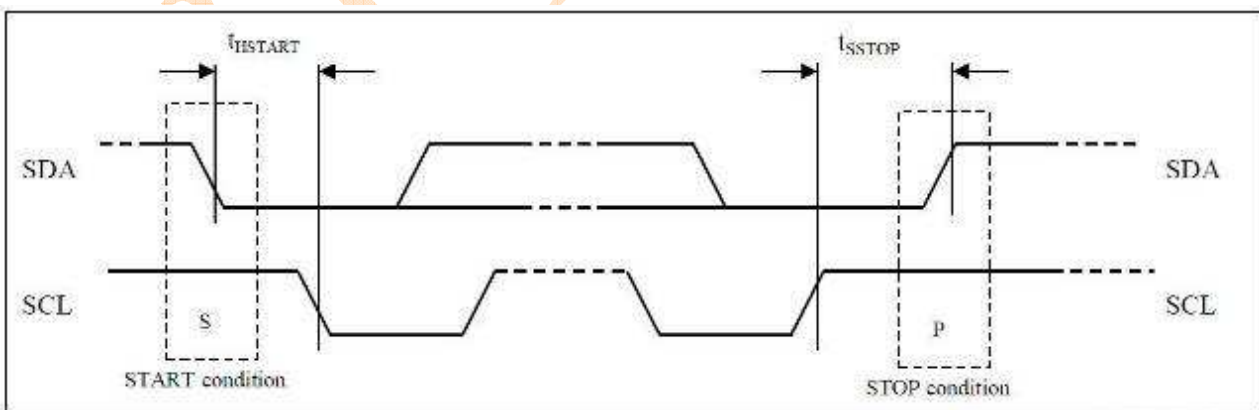
The I²C-bus interface gives access to write data and command into the device.

The write mode of I²C-bus in chronological order.



Definition of the Start and Stop Condition

1. The master device initiates the data communication by a start condition. The definition of the start condition. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH

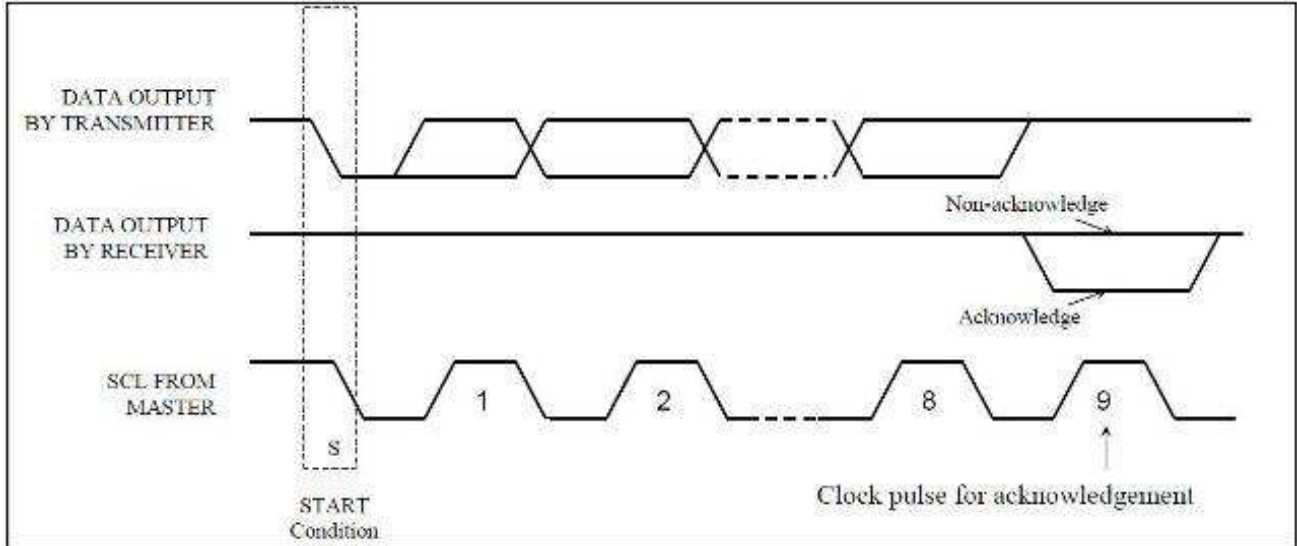


2. The slave address is following the start condition for recognition use. For the SSD1311, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3. The write mode is established by setting the R/W# bit to logic “0”.

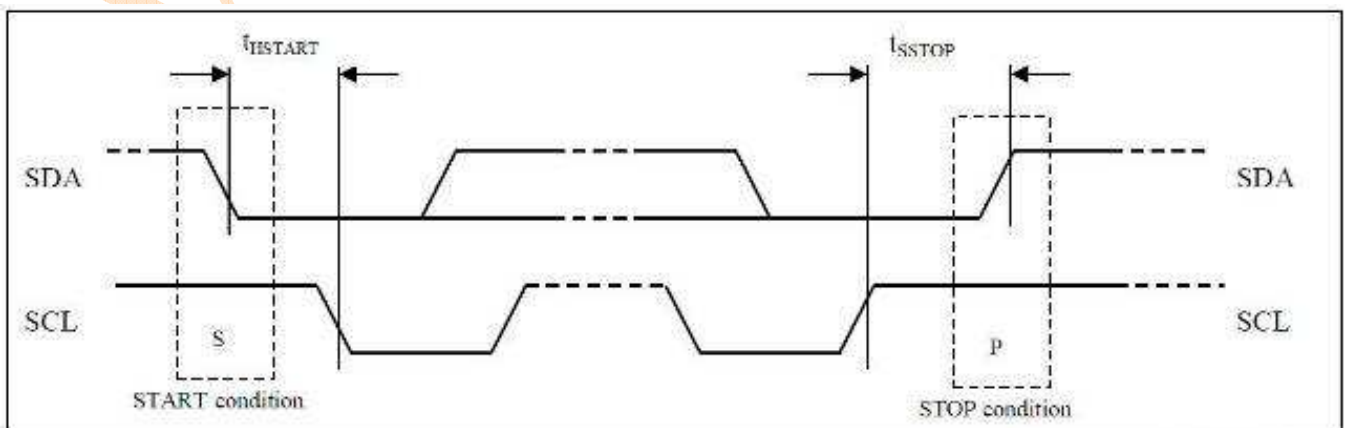
Defintion of the acknowledgement condition

1. An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.

The graphical representation of the acknowledge signal.



2. After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0"s.
 - a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
 - b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
3. Acknowledge bit will be generated after receiving each control byte or data byte.
4. The write mode will be finished when a stop condition is applied. The stop condition is also defined. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the SCL" stays HIGH.

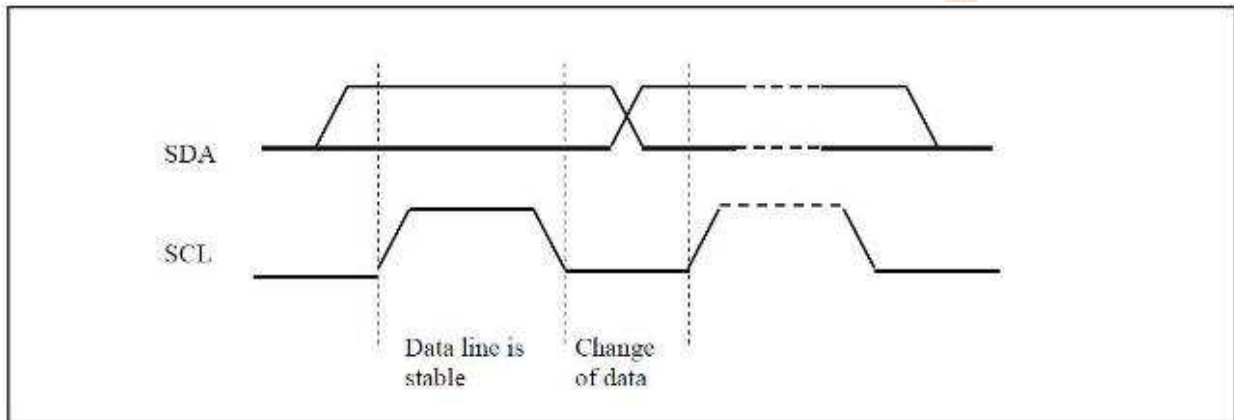


Definition of the data transfer condition

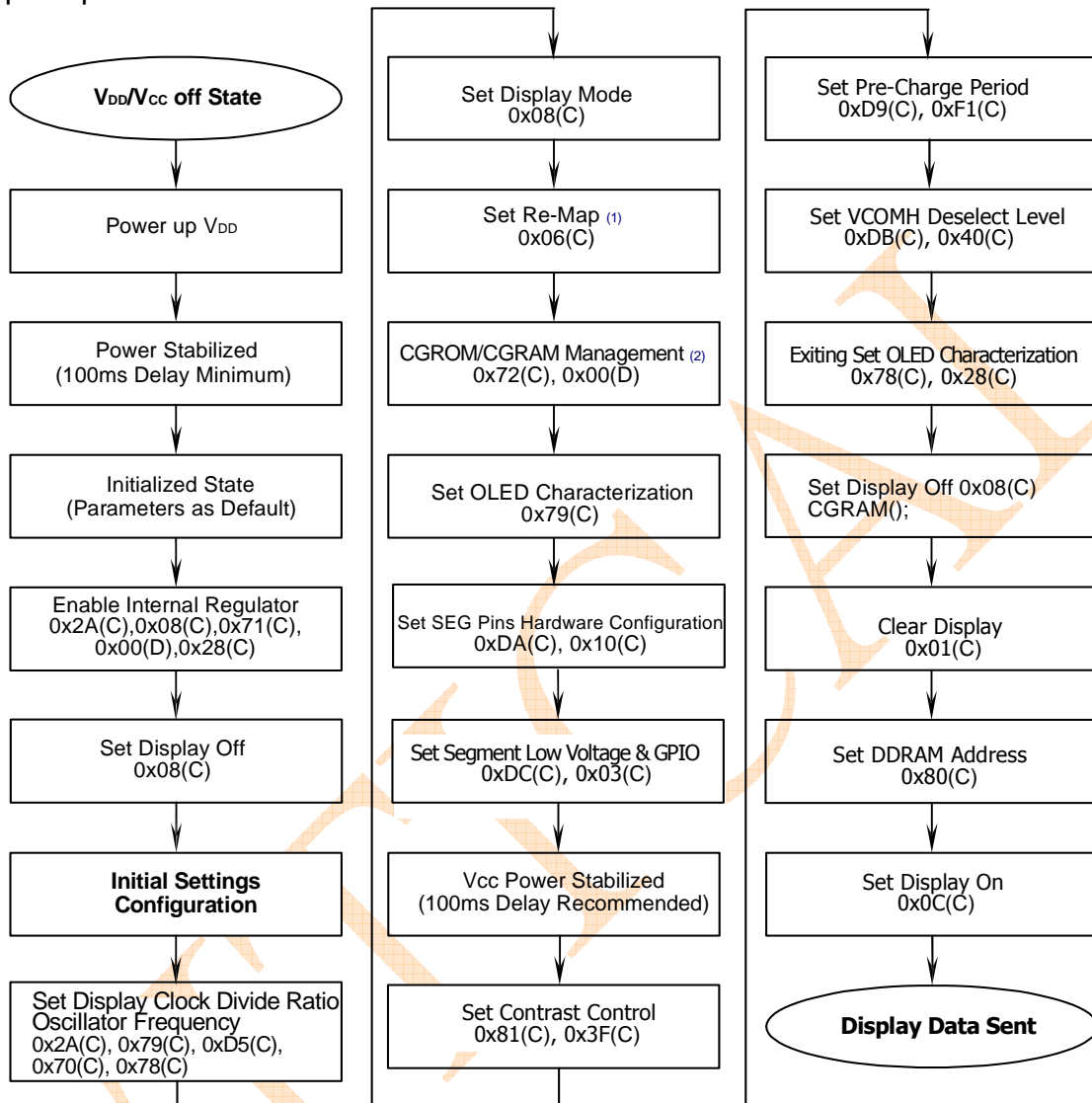
Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

The graphical representation of the data transfer.



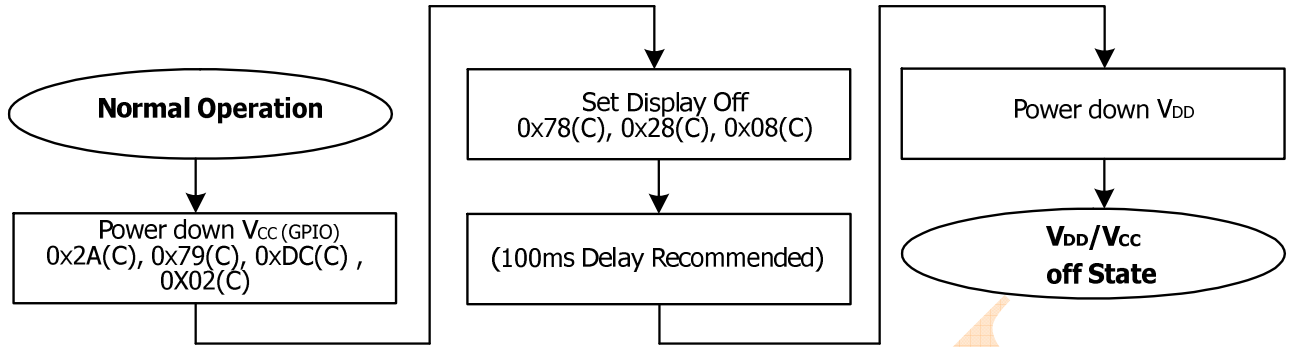
<Power up Sequence>



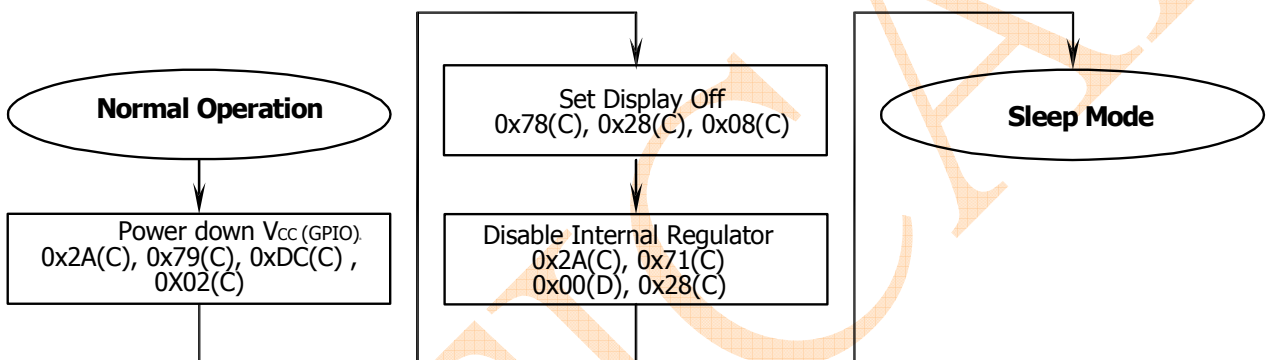
※ (C) : Write Command

※ (D) : Write Data

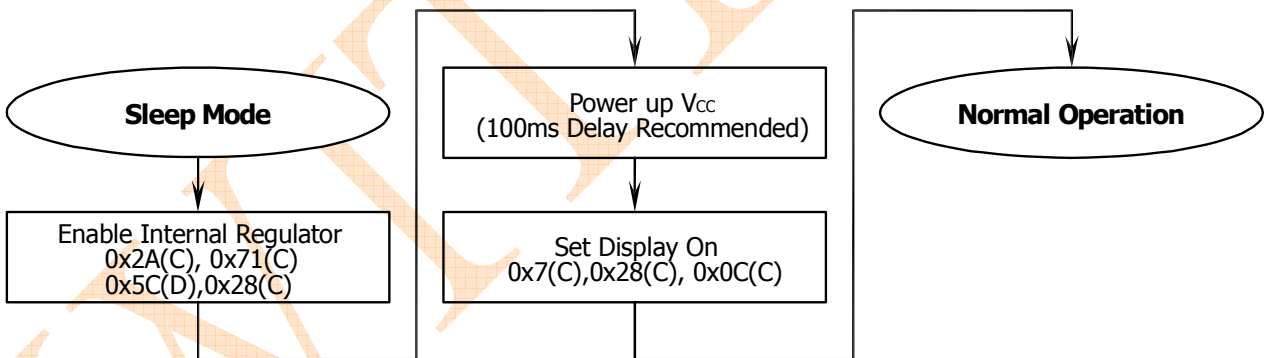
If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.



<Entering Sleep Mode>



<Exiting Sleep Mode>



(13)SSD1311 CGROM CHARACTER CODE

ROMA(Default)- English + Euro + Block Elements + Miscellaneous Dingbats

b7-4 \ b3-0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0001	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0010	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0011	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0100	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0101	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0110	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0111	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1000	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1001	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1010	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1011	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1100	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1101	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1110	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1111	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

b7-4 \ b3-0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
0001	♣	♠	♣	♠	♣	♠	♣	♠	♣	♠	♣	♠	☐	☐	☐	☐
0010	!	"	#	\$	%	&	'	()	*	+	,	-	.	/	
0011	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
0100	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
0101	Ð	Ñ	Ò	Ó	Ô	Õ	Ö	×	Ý	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
0110	à	á	â	ã	ä	å	æ	ç	è	é	ê	ë	ì	í	î	ï
0111	ª	«	»	¼	½	¾	¿	À	Á	Â	Ã	Ä	Å	Æ	Ç	È
1000	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
1001	Ð	Ñ	Ò	Ó	Ô	Õ	Ö	×	Ý	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
1010	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
1011	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
1100	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
1101	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
1110	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
1111	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï

b7-4 \ b3-0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	¡	¢	£	¤	¥	¦	§	¨	©	ª	«	¬	®	¯	°	±
0001	²	³	´	µ	¶	·	¸	¹	º	»	¼	½	¾	¿	À	Á
0010	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï	Ð	Ñ
0011	Ò	Ó	Ô	Õ	Ö	×	Ø	Ù	Ú	Û	Ü	Ý	Þ	ß	à	á
0100	â	ä	å	æ	ç	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò
0101	ó	ô	õ	ö	÷	ø	ù	ú	û	ü	ý	þ	ß	à	á	â
0110	ä	å	æ	ç	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò	ó
0111	ô	õ	ö	÷	ø	ù	ú	û	ü	ý	þ	ß	à	á	â	ã
1000	ã	ä	å	æ	ç	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò
1001	ä	å	æ	ç	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò	ó
1010	å	æ	ç	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò	ó	ô
1011	æ	ç	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò	ó	ô	õ
1100	ç	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò	ó	ô	õ	ö
1101	è	é	ê	ë	ì	í	î	ï	ð	ñ	ò	ó	ô	õ	ö	÷
1110	é	ê	ë	ì	í	î	ï	ð	ñ	ò	ó	ô	õ	ö	÷	ø
1111	ê	ë	ì	í	î	ï	ð	ñ	ò	ó	ô	õ	ö	÷	ø	ù

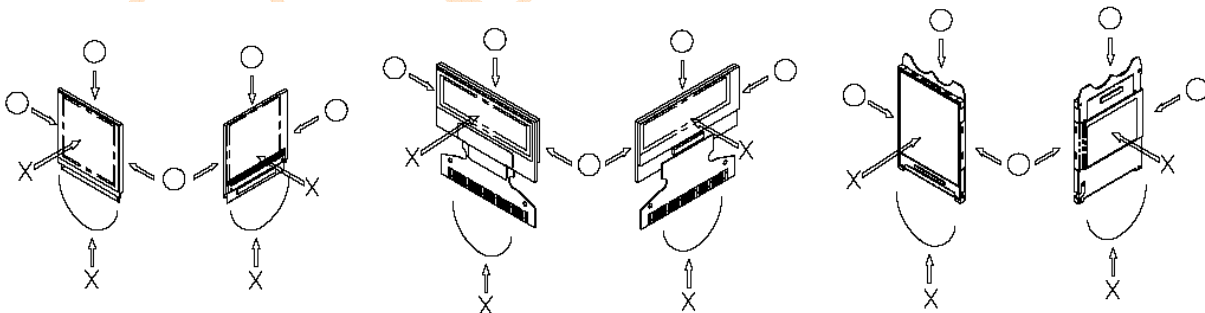
(14)Precautions in use of OLED Modules-1

Modules

- (1) Avoid applying excessive shocks to module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED module.
- (3) Don't disassemble the OLED Module.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist OLED Module.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

Handling Precautions

- (1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- (2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- (3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- (4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
- (5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
 - * Scotch Mending Tape No. 810 or an equivalent
 Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:
 - * Water
 - * Ketone
 - * Aromatic Solvents
- (6) Hold OLED display module very carefully when placing OLED display module into the System housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- (7) Do not apply stress to the LSI chips and the surrounding molded sections.
- (8) Do not disassemble nor modify the OLED display module.
- (9) Do not apply input signals while the logic power is off.
- (10) Pay sufficient attention to the working environments when handing OLED display

modules to prevent occurrence of element breakage accidents by static electricity.

- * Be sure to make human body grounding when handling OLED display modules.
- * Be sure to ground tools to use or assembly such as soldering irons.
- * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.

- (11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5.
- (12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

Storage Precautions

- (1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments.

(We recommend you to store these modules in the packaged state when they were shipped from Witical Technology Inc.

At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

- (2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

Designing Precautions

- (1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
- (2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- (3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- (4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- (5) As for EMI, customer may take necessary measures on the equipment side basically.
- (6) When fastening the OLED display module, fasten the external plastic housing section.
- (7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

- * Connection (contact) to any other potential than the above may lead to rupture of the IC.

(15)Precautions in use of OLED Modules-2

- (1) Avoid applying excessive shocks to module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED module.
- (3) Don't disassemble the OLED Module.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist OLED Module.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

Precautions when disposing of the OLED display modules

- (1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

Other Precautions

- (1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- (2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
 - * Pins and electrodes
 - * Pattern layouts such as the TCP & FPC
- (3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
 - * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
 - * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.
- (4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- (5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.
- (6) Resistors, capacitors and other passive components will have different appearance and color caused by the different supplier.
- (7) Our company will have the right to upgrade and modify the product function.