WLRS-590 Series

LoRa IoT Module

Low Power Wide Area Network Solution

The WLRS-590 is designed & manufactured in a smallest form factor -SiP (System in Package). The WLRS-590 integrates with Semtech SX1276 and a 32-bit ultra-low power Cortex M0+ MCU (STM32L073x).

The WLRS-590 is a general purpose SiP for sensor integration. Sensor vendors can speed up their LPWAN integration by embedding this SiP in their design. The WLRS-590 can achieve a sensitivity of over -137dBm. The high sensitivity combined with the integrated +20dBm power amplifier yields industry leading link budget marking it optimal for any low data rate application requiring range or robustness.

The WLRS-590 is based on LoRa technology to provides low power long range high sensitivity communication using spread spectrum. The WLRS-590 also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference immunity and energy consumption. WLRS-590 module provides a commands set interface that can use LoRa and LoRaWAN communication through UART interface.

Key Feature :

- Programmable bit rate up to 37500 bps
- High sensitivity down to -137 dBm
- Preamble detection
- Embedded memories (up to 192k bytes of Flash memory and 20k bytes of RAM)
- 3x UART
- Small foot print: 13mm x 11mm x 1.1mm

Application:

- Automated Meter Reading
- Intelligent tracking
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Long range Irrigation Systems
- Forest fire detection
- Healthcare Application

Specification :

MCU	STM32L073xZ ARM Coretex-M0+ 32-bit
Chipset	Semtech SX1276
Frequency	EU 863-870 MHz ISM Band US 902-928 MHz ISM Band AS923 MHz ISM Band (Japan 920-928 MHz)
Flash memory / RAM	192k bytes / 20k bytes
Form factor	SiP
Interface	UART, SPI, I2C, USB,ADC
Antenna	External
Transmitter Power	20dBm
Receive Sensitivity	-137 dBm
Temperature	-40°C to + 85°C(Operating) -50°C to + 105°C(Storage)
Humidity	Operating: 10~95% (No-Condensing) Storage: 5~95% (No-Condensing)
Input Voltage	3.3V
Package	Molding type with LGA landing
Dimension	L:13mm x W:11mm x H:1.1mm

Product Version

Detail in the flowing table

Frequency Range	Spreading Factor	Bandwidth (K Hz)	Effective Bitrate (bps)	Est. Sensitivity (dBm)
863-870MHz 902-928 MHz	6-12	62.5 - 500	146 - 37500	-109 to -137

LoRa setting SF=12, BW=62.5k, Long-Range Mode, highest LNA gain, LnaBoost for Band 1.

Optional FW support for European band 868MHz

Electrical Characteristics

Absolute Maximum Ratings

Symbo	Parameter	Min	Typ.	Max.	Unit
VDD33	Supply Voltage	-0.3		3.9	v
VIN	Input voltage on digital pins	-0.3		3.9	v
Pmr	RF Input Level			+10	10dBm

Recommended Operating Range

Symbo	Parameter	Min.	Typ.	Max.	Unit
VDD33	Supply Voltage	2.4	3.3	3.6	V
ML	RF Input Level			+10	dBm

Power Consumption Characteristics

Symbo	Parameter	Conditions	Typ.	Max.	Unit
IDDSL	Supply current in Sleep mode	Sleep stop Mode		5	uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	9	9.6	mA
IDDR	Supply current in Receive mode		17.5		mA
IDDT	Supply current in Transmit mode with impedance matching	RFOP= +20 dBm RFOP= +17 dBm RFOP= +13 dBm RFOP= +7 dBm	127 82 65 49		mA

RF Characteristics

The table gives the electrical specifications for the transceiver operating with LoRa Modulation

Supply voltage	3.3V
Temperature	25℃
Frequency bands	915/868 MHz
Bandwidth(BW)	125 KHz
Spreading Factor(SF)	12
Error Correction Code (EC)	4/6
Packet Error Rate (PER)	1%
Output power	13 dBm in transmission
CRC on payload	enabled
Payload length	64 bytes
Preamble Length	12 symbols (programmed register preamblength=8)
With matched impedances	

LoRa Transmitter (Conductive)					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Frequency Range	Band 1	863	915	928	MHz
Tx Power Level	PA_BOOST pin	18.0	19.5	21.0	dBm
LoRa Receiver (Conductive)					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Frequency Range	Band 1	863	915	928	MHz
RFS_L62_HF (Long-Range Mode, highest LNA gain, LNAboost, 62.5 kHz bandwidth)	SF = 6 SF = 7 SF = 8 SF = 12		-119 -114 -127 -137		dBm dBm dBm dBm
RFS_L500_HF (Long-Range Mode, highest LNA gain, LNA boost, 500 kHz bandwidth)	SF = 6 SF = 7 SF = 8 SF = 9 SF = 10 SF = 11 SF = 12		-109 -114 -117 -120 -123 -126 -128		dBm dBm dBm dBm dBm dBm dBm

Digital Characteristics

DC characteristics

Input voltage levels

Symbol	Description	Conditions	Min	Typ.	Max	Unit
VIH	I/O input high level voltage	NRST	0.7xVDD33	-	-	v
		BOOT0	0.7xVDD33	-	-	v
		GPIO	0.7xVDD33	-	-	v
VIL	I/O input low level voltage	NRST	-	-	0.3xVDD33	v
		BOOT0	-	-	0.14xVDD33	v
		GPIO	-	-	0.3xVDD33	v
R_{PU}	Weak pull-up Equivalent resistor	V_{IN} = GND	30	45	60	KΩ
R_{PD}	Weak pull-down Equivalent resistor	V_{IN} = VDD33	30	45	60	KΩ

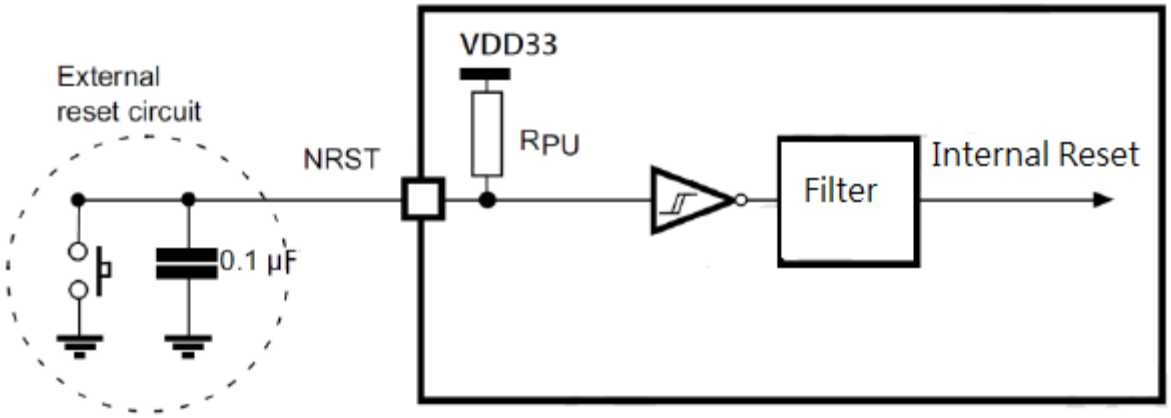
Output voltage levels

Symbol	Description	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port /IIO=+8mA 2.7V≦VDD33≦3.6V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		VDD33-0.4	-	V
V_{OL}	Output low level voltage for an I/O pin	TTL port / IIO =+8 mA 2.7V≦VDD33≦3.6V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin	TTL port / IIO = -6 mA 2.7V≦VDD33≦3.6V	2.4	-	V
V_{OL}	Output low level voltage for an I/O pin	IIO = + 15 mA 2.7V≦VDD33≦3.6V	-	1.3	V
V_{OH}	Output high	IIO = - 15 mA	VDD33-1.3	-	V

	level voltage for an I/O pin	2.7V≦VDD33≦3.6V			
V_{OL}	Output low level voltage for an I/O pin	IIO = + 4 mA 1.65 V≦VDD33≦3.6V	-	0.45	V
V_{OH}	Output high level voltage for an I/O pin	IIO = + 4 mA 1.65 V≦VDD33≦3.6V	VDD33-0.45	-	V

NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor (R_{PU})
The following figure is recommended NRST pin protection circuit against parasitic resets.



Symbol	Description	Conditions	Min	Typ.	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		VSS		0.8	V
$V_{IH(NRST)}$	NRST input high level voltage		1.4		VDD33	V
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 2 mA 2.7V < VDD33<3.6V			0.4	V
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 1.5 mA 1.65V < VDD33<2.7V			0.4	V
$V_{hys(NRST)}$	NRST Schmitt			10%		mV

	trigger voltage hysteresis			VDD33		
R_{PU}	Weak pull-up Equivalent resistor	V_{IN} = GND	30	45	60	KΩ
V_F	NRST Input filtered pulse				50	nS
V_{NF}	NRST Input not filtered pulse	VDD33 > 2.7V		350		nS

UART Interface Parameters

Baud Rate = 38400 bps
Data Bits = 8 bits
Stop Bits = 1 bit
Parity Check = None
Flow Control = None

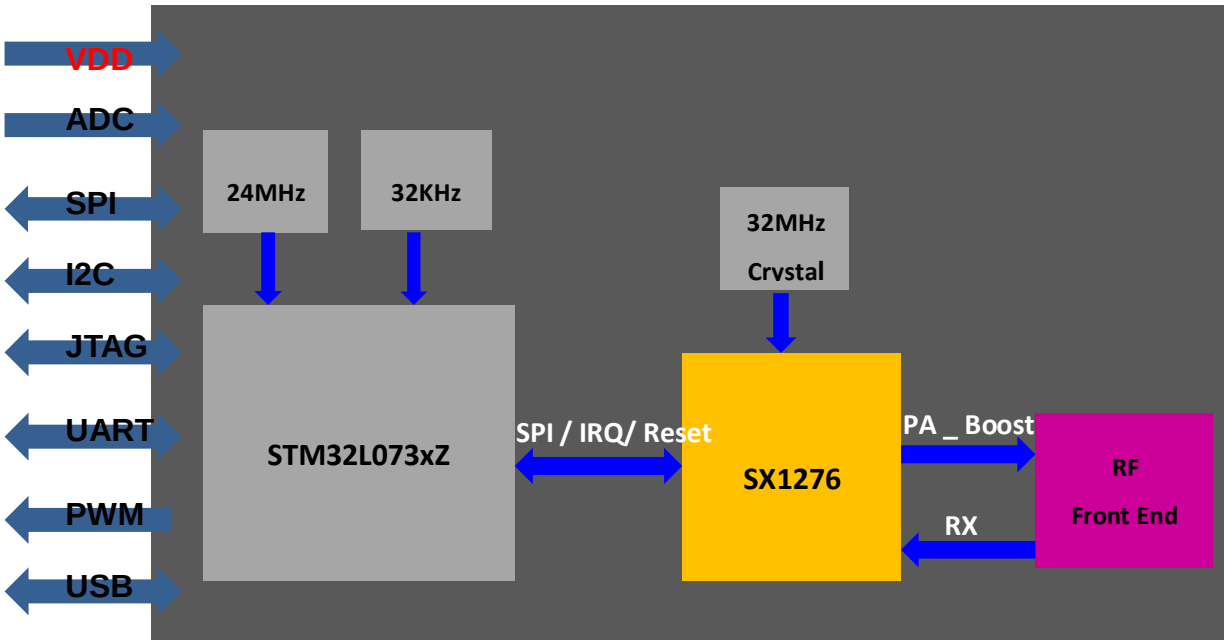
Pin Definition

Pin	Definition	I/O	Description
1	NC		
2	GND		Ground pin
3	GND		Ground pin
4	PC0	I/O	MCU pin name: PC0
5	PC1	I/O	MCU pin name: PC1
6	PC2	I/O	MCU pin name: PC2
7	PC3	I/O	MCU pin name: PC3
8	NC		
9	NC		
10	NC		
11	NC		
12	NRST		Hardware reset pin
13	PA0	I/O	MCU pin name: PA0
14	GND		Ground pin
15	GND		Ground pin

16	PA2_UART2_TX	I/O	MCU pin name: PA2
17	PA3_UART2_RX	I/O	MCU pin name: PA3
18	PA4_SPI1_NSS	I/O	MCU pin name: PA4
19	PA5_SPI1_SCK	I/O	MCU pin name: PA5
20	PA6_SPI1_MISO	I/O	MCU pin name: PA6
21	PA7_SPI1_MOSI	I/O	MCU pin name: PA7
22	PC4	I/O	MCU pin name: PC4
23	PC5	I/O	MCU pin name: PC5
24	PB0_IO_INT1	I/O	MCU pin name: PB0
25	PB0_IO_INT2	I/O	MCU pin name: PB1
26	PC6	I/O	MCU pin name: PC6
27	PC7	I/O	MCU pin name: PC7
28	PC8	I/O	MCU pin name: PC8
29	PC9	I/O	MCU pin name: PC9
30	RXTX/RFMOD	O	Control signal from SX1276, which connects to internal RF switch at the same time
31	GND		Ground pin
32	GND		Ground pin
33	RF_ANT	I/O	RF I/O
34	GND		Ground pin
35	GND		Ground pin
36	PA1_RF_FEM_CPS	I/O	MCU pin name: PA1
37	GND		Ground pin
38	NC		
39	GND		Ground pin
40	NC		
41	GND		Ground pin
42	NC		
43	VDD33		Power Supply
44	VDD33		Power Supply
45	PA8_USART1_CK	I/O	MCU pin name: PA8
46	PA10_USART1_RX	I/O	MCU pin name: PA10
47	PA9_USART1_TX	I/O	MCU pin name: PA9
48	PA11_USART1_CTS	I/O	MCU pin name: PA11
49	PA12_USART1_RTS	I/O	MCU pin name: PA12
50	PA13_SWDIO		Serial wire(SWD) debug interface
51	PA14_SWCLK		Serial wire(SWD) debug interface

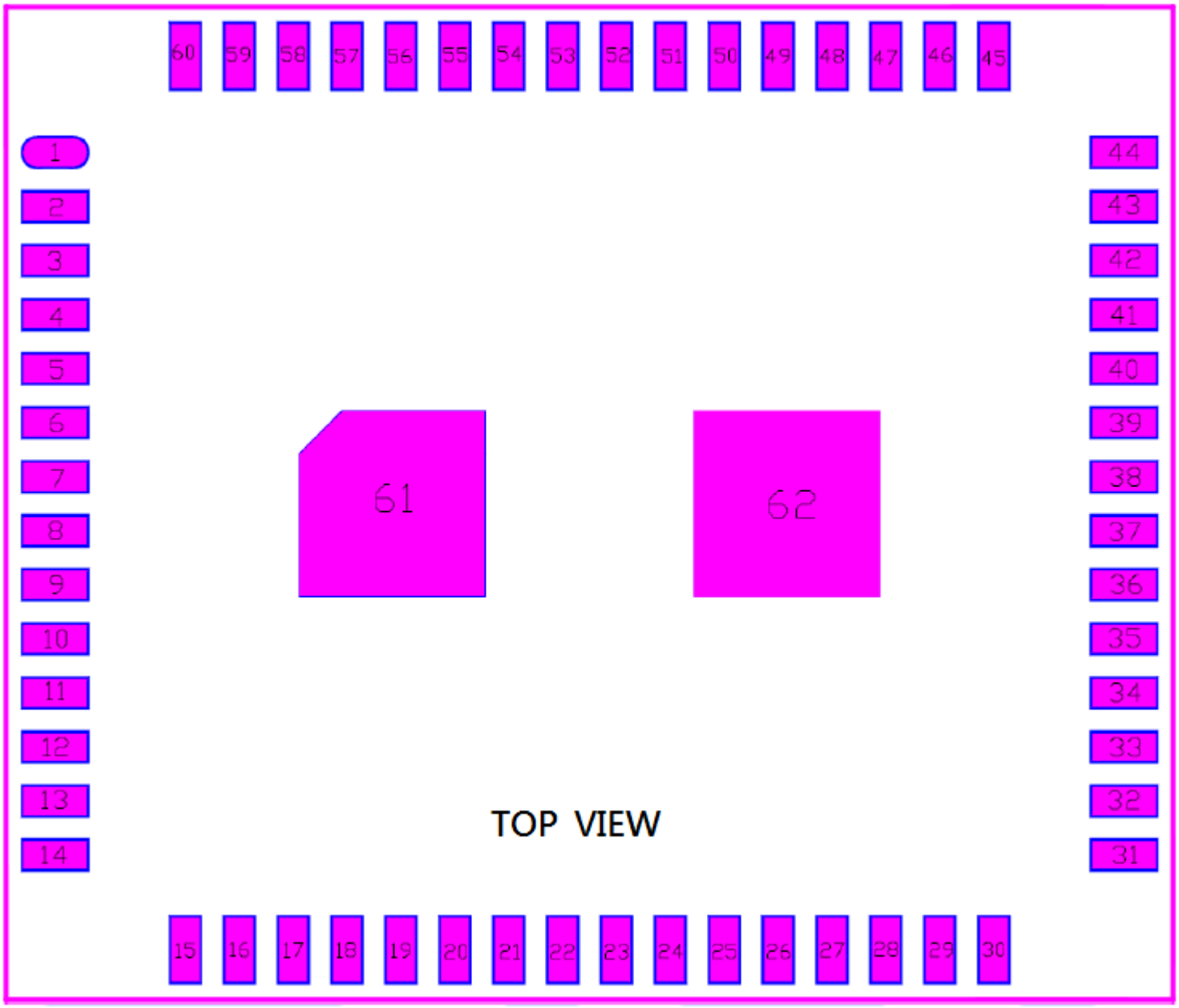
52	PC10	I/O	MCU pin name: PC10
53	PC11	I/O	MCU pin name: PC11
54	PC12	I/O	MCU pin name: PC12
55	PD2	I/O	MCU pin name: PD2
56	PB5	I/O	MCU pin name: PB5
57	PB6_I2C1_SCL	I/O	MCU pin name: PB6
58	PB7_I2C1_SDA	I/O	MCU pin name: PB7
59	BOOT0	I	Boot mode selection pin
60	PB8_IO_LED_FCT	I/O	MCU pin name: PB8
61	GND		Ground pin
62	GND		Ground pin

Block Diagram



Pin Assignment

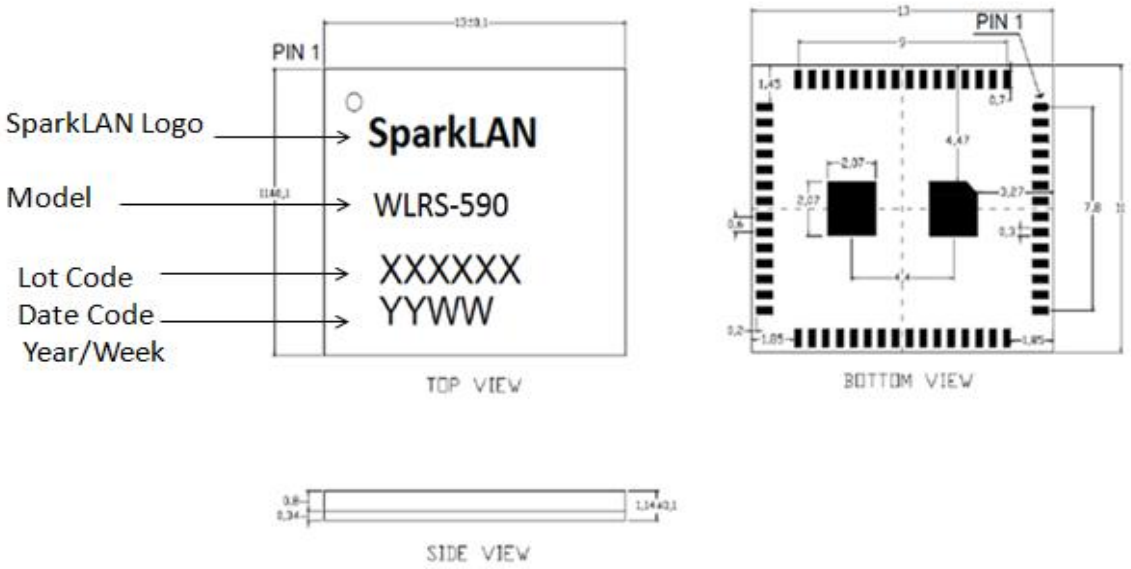
The SiP module will conform to the following pin map, shown in the following diagram (top view)



Mechanical Dimension

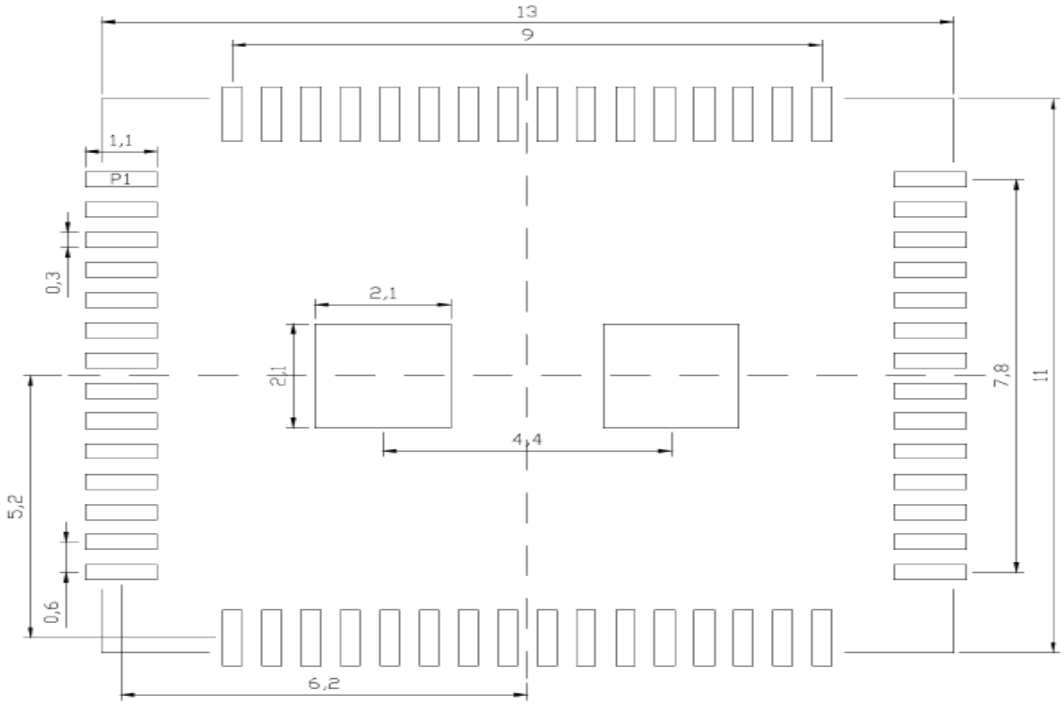
Unit: mm

13mm X 11mm X 1.1mm



Recommended Footprint

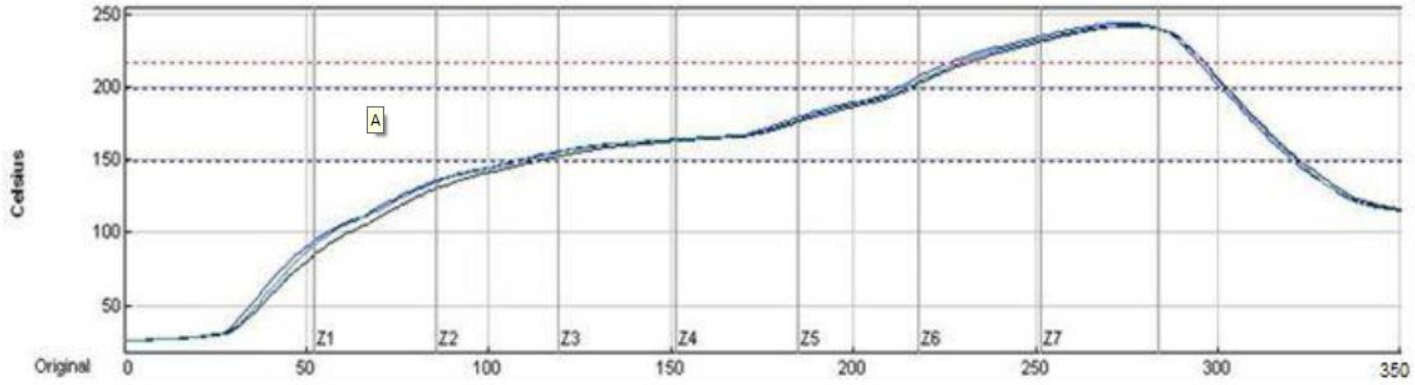
Unit: mm



TOP View

Recommended Reflow Profile

Reflow Profile for SiP on board Assembly



Preheat time	150℃-200℃ ：105+/-15 sec
Dwell Time	Over 220℃ ：70+5/-10 sec
Peak Temp	240 +10/-5℃
Ramp UP/Down Rate	UP：3+0/-2℃ / sec Down：2+0/-1℃ /sec

SiP Module Preparation

Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transport and storage with anti -static tray and packing. This protective package must be remained in suitable environment until the module is assembled and soldered onto the main board.

SMT Preparation

1. Calculated shelf life in sealed bag: 6 months at<40℃ and <90% relative humidity (RH).
2. Peak package body temperature: 250℃.

3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must.

A. Mounted within: 168 hours of factory conditions<30℃/60%RH.

B. Stored at≦ 10%RH with N2 flow box.

4. Devices require baking, before mounting, if:

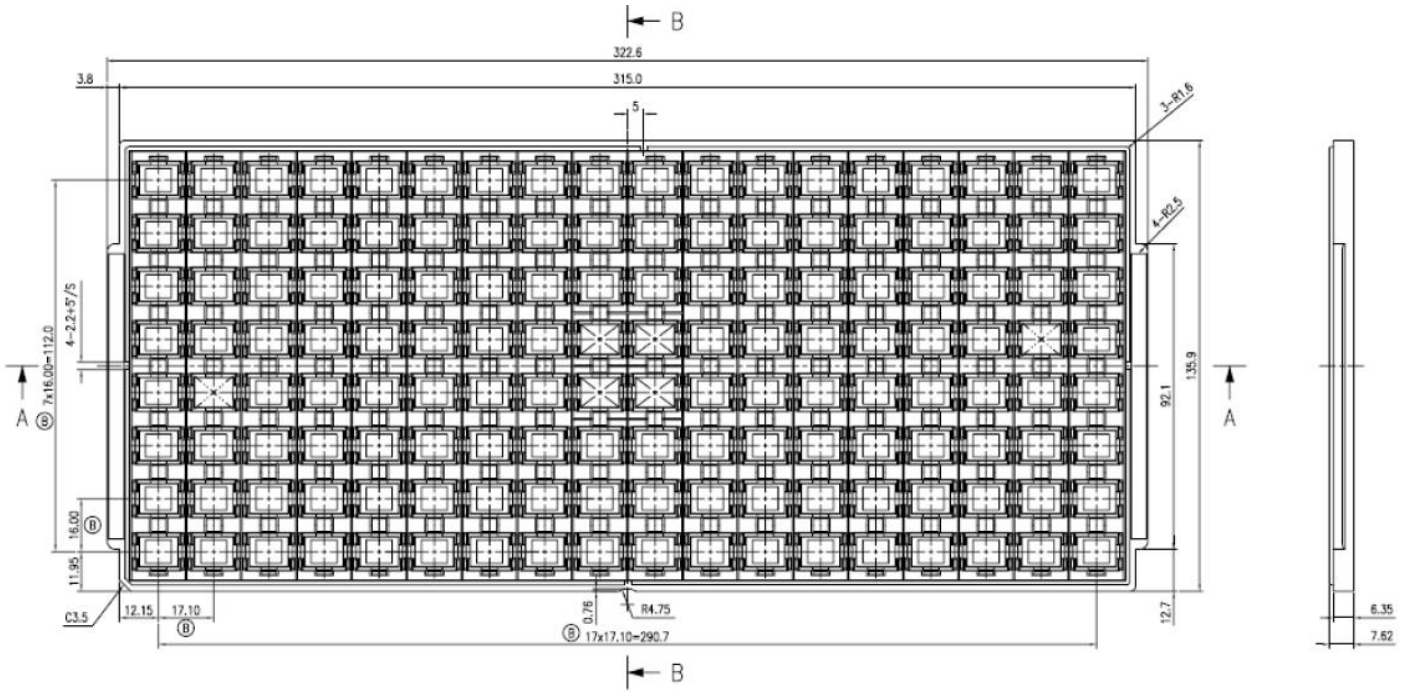
A. Package bag does not keep in vacuumed while first time open.

B. Humidity Indicator Card is >10% when read at 23±5℃.

C. Expose at 3A condition over 8 hours or Expose at 3B condition over 24 hours.

5. If baking is required, devices may be baked for 12 hours at 125±5℃.

Tray Dimension



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