PiTek

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CUSTOMER APPROVAL SHEET

Company Name

MODEL **PA320320A**

CUSTOMER **Title :**

APPROVED **Name :**

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.)**

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Product Specification

1.63" COLOR AMOLED MODULE

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	Mar. 5, 2014		First Draft
1.0	Mar.18,2014	17 21 22 23	Revise H. Specifications_Optical characteristics Add I. Reliability test items_Vibration test Add J.packing Revise K.2D/3D drawing;
2.0	Apr.16,2014	7 11 14, 15 16 24	Add Idle power consumption & revise panel power Revise TE description Revise Initial Code for display optimization B500=0x05 -> 0x03; B501=0x05 -> 0x03; B502=0x05 -> 0x03 BA00=0x13 -> 0x03; BA01=0x13 -> 0x03; BA02=0x13 -> 0x03 BE00=0x22 -> 0x32 Revise CF description Revise K. 2D drawing
3.0	July.3,2014	24	Revise K. 2D drawing
4.0	July.17,2014	24	Revie 2D drawing for foam tape modified.
5.0	Aug.7,2014	25	Add Precaution
6.0	Oct. 6,2014	 13 14 15 24	Revise Initial Code for display optimization BD00~BD04 =0x03 20 14 4B 00 BE00~BE04 =0x03 20 14 4B 01 BF00~BF04 =0x03 20 14 4B 00 EB00=0x02 E900~E902 = 0x00 36 38 B600=0x53 -> 0x55; B601=0x53 -> 0x55; B602=0x53 -> 0x55 B700=0x33 -> 0x36; B701=0x33 -> 0x36; B702=0x33 -> 0x36 CF03=0xEF -> 0XE8 Revie 2D drawing for foam tape modified.
7.0	Sep. 21,2015	15~17	Update initial code.
8.0	Oct. 16, 2015	19	Adding Idle mode flow.
9.0	Jan.12,2016	13 18	Update initial code. Remove “others” column. Update step 9 of brightness control to E8.
10.0	Mar.15,2016	7	Update Note 4. VCI Current must < 9mA at Idle mode.
11.0	May.06,2016	17	Update Power off sequence.

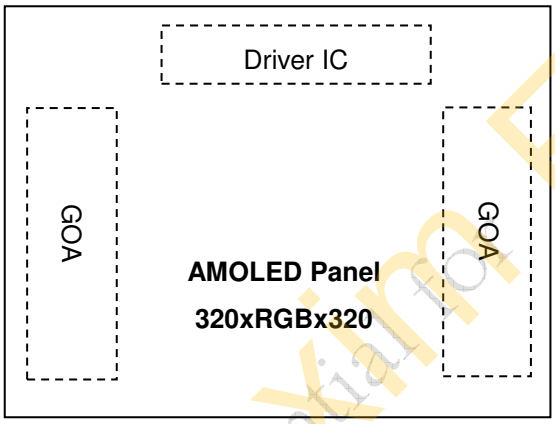
Contents

A. General Specification

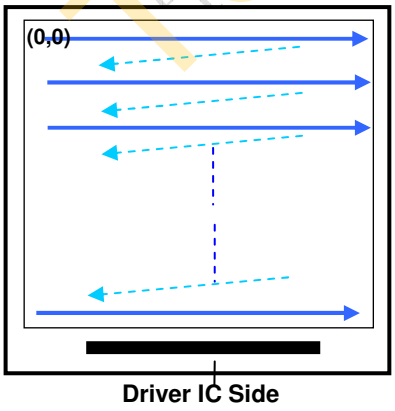
1. Physical Specifications

	Item	Description	Remark
1	Screen Size (inch)	1.63”	
2	Display Mode	AMOLED	
3	Display Resolution (dot)	320xRGBx320	
4	Active Area (mm*mm)	29.28 (H)×29.28(V)	
5	Pixel Configuration	Hyper R.G.B	
6	Display Color (M)	16.7	
7	Brightness (nits)	300	
8	Interface	MIPI DSI	
9	Outline Dimension (mm*mm*mm)	32.08 (H) × 36.48(V) × 0.7(T)	cell+foam

2. Module Block Diagram



3. Panel Scan direction



B. Electrical Specifications

1. Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interface

Recommended connector: AXE520127 (Panasonic)

FPC	Pin_name	I/O	Description
1	**ELVSS**	P	AMOLED power Negative
2	**ELVSS**	P	AMOLED power Negative
3	**ELVSS**	P	AMOLED power Negative
4	**VDD**	P	Power supply for analog
5	**IOVDD**	P	Power supply for Interface system excep MIPI interface
6	**GND**	P	GND
7	**TE**	O	Vsync(vertical sync)signal output from panel to avoid tearing effect
8	**MTP**	I	MTP(need to indicate to connect GND or NC)
9	**RESX**	I	Device reset signal (0 : Enable ; 1: Disable)
10	**SWIRE**	O	SWIRE signal for PWR IC control
11	**ELVDD**	P	AMOLED power positive
12	**ELVDD**	P	AMOLED power positive
13	**ELVDD**	P	AMOLED power positive
14	**GND**	P	GND
15	**DSI_D0N**	I/O	MIPI data negative signal
16	**DSI_D0P**	I/O	MIPI data positive signal
17	**GND**	P	GND
18	**DSI_CLKN**	I	MIPI strobe negative signal
19	**DSI_CLKP**	I	MIPI strobe postive signal
20	**GND**	P	GND

Note: I = input ; O = output ; P = Power ; I/O = input / Output

2. Absolute maximum ratings

Item	Symbol	Min.	Max.	Unit	Remark
Digital Power supply	IOVDD	-0.3	5.5	V	
Analog Power supply	VDD	-0.3	5.5	V	
ELVDD power supply	ELVDD	-	5.0	V	
ELVSS power supply	ELVSS	-5.0	-	V	

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

C. Electrical Characteristics

1. DC Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power supply		IOVDD	1.65	1.8	1.95	V	Note1
Analog Power supply		VDD	2.8	3.0	3.1	V	Note1
ELVDD power supply		ELVDD	4.57	4.60	4.63	V	Note1,2
ELVSS power supply		ELVSS	-3.35	-3.40	-3.45	V	Note1
Input Signal Voltage	H Level	V_{IH}	0.8*IOVDD	-	IOVDD	V	Note1
	L Level	V_{IL}	0	-	0.2*IOVDD	V	
Output Signal Voltage	H Level	V_{OH}	0.8*IOVDD	-	IOVDD	V	Note1
	L Level	V_{OL}	0	-	0.2*IOVDD	V	Note1

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note 2 : TPS65631W Positive output voltage = 4.6V ± 0.8% at -40℃ ≦ Ta ≦ +85 ℃

2. Display Current Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power		P_{NL}	ELVDD:4.6V ELVSS:-3.4V	--	--	138.4	mW	Note1,2,
		I_{NL}		--	--	17.3	mA	Note1,2,
IC	**Normal**	P_{VDD}	VDD : 3.0V	--	25.2	39.3	mW	Note2,
		I_{VDD}		--	8.4	13.1	mA	Note2,
		P_{IOVDD}	IOVDD :1.8V	--	18.0	19.8	uW	Note2,
		I_{IOVDD}		--	10.0	11.0	uA	Note2,
	Idle	P_{VDD}	VDD : 3.0V	--	12.0	15.3	mW	Note3,4
		I_{VDD}		--	4.0	5.1	mA	Note3,4
		P_{IOVDD}	IOVDD :1.8V	--	18.0	19.8	uW	Note3,
		I_{IOVDD}		--	10.0	11.0	uA	Note3,

Note 1: Based on L255 (300nits) full white pattern

Note 2: Testing in MIPI-DSI frame rate 60Hz CMD mode.

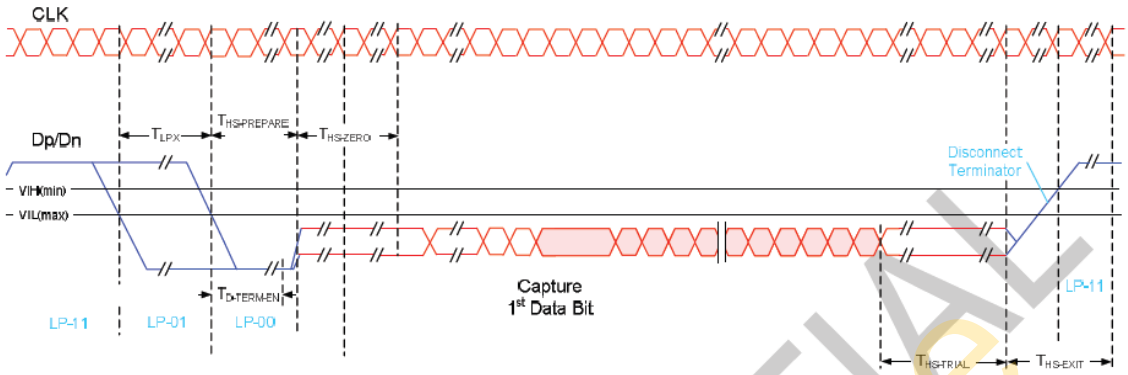
Note 3: Testing in MIPI-DSI frame rate 30Hz CMD mode.

Note 4: VCI Current must < 9mA at Idle mode.

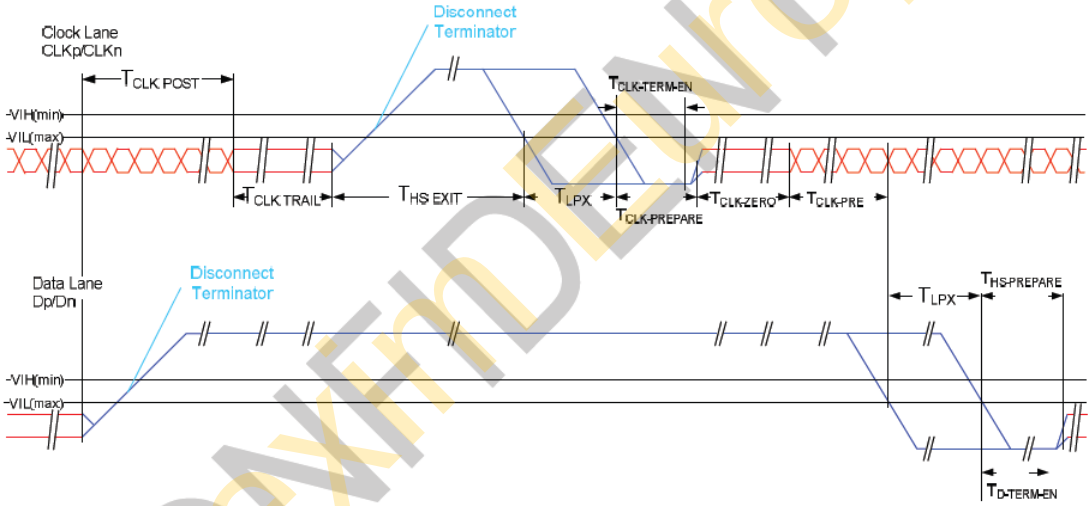
D. AC Characteristics

1. MIPI Interface Characteristics

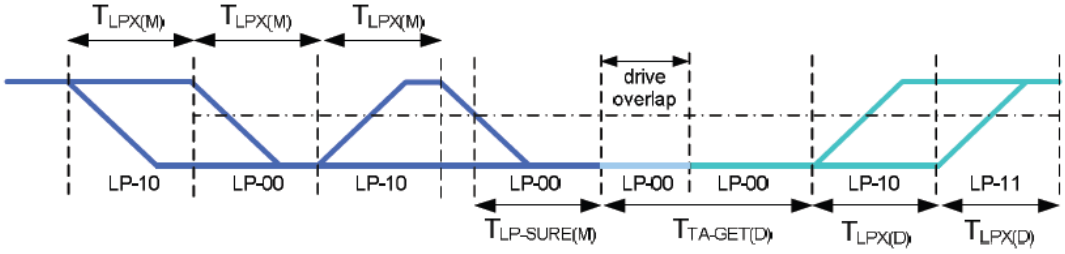
HS Data Transmission Burst



HS clock transmission



Turnaround Procedure



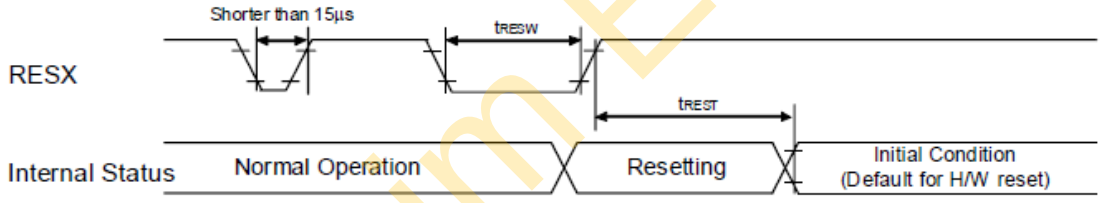
Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		60 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	96*UI			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state	100		150	ns

	period of MCU to display module				
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX(D)}$			ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX(D)}$			ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns

2. Display RESET Timing Characteristics

Reset input timing



IOVDD=1.65 to 1.95V, VDD=2.8 to 3.1V, AGND=DGND=0V, Ta=-40 to 85℃

Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	15	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

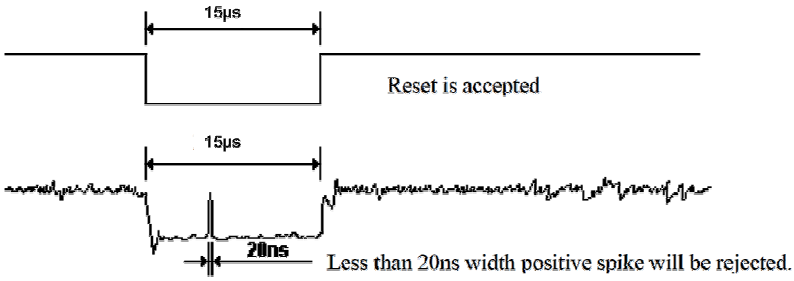
RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 15µs	Reset
Between 5µs and 15µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display

remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

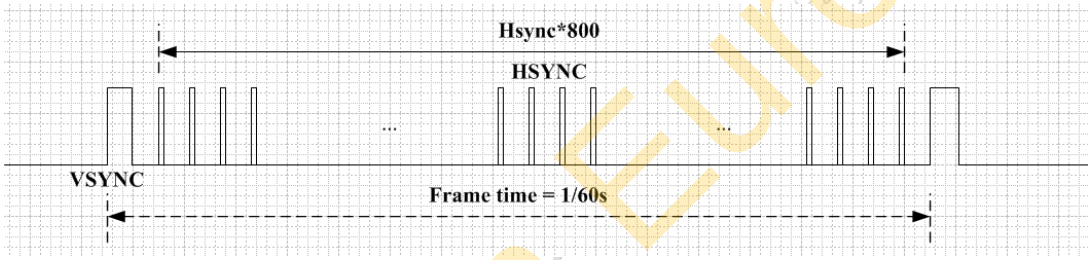
Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

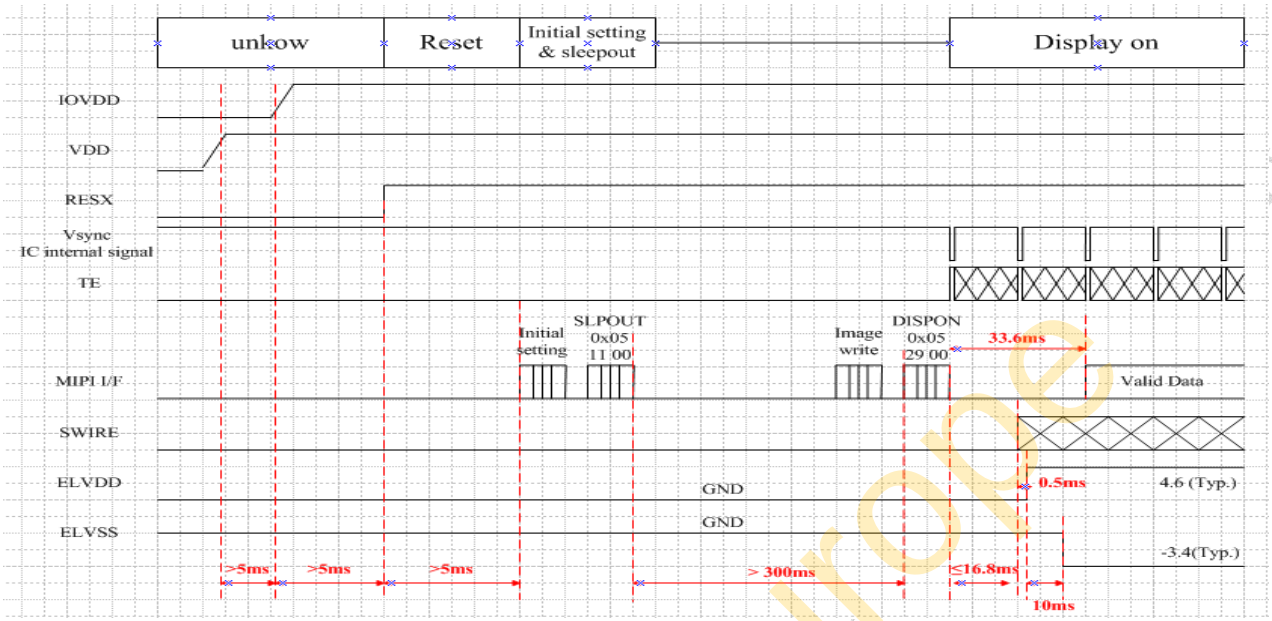
3. TE Timing Characteristics



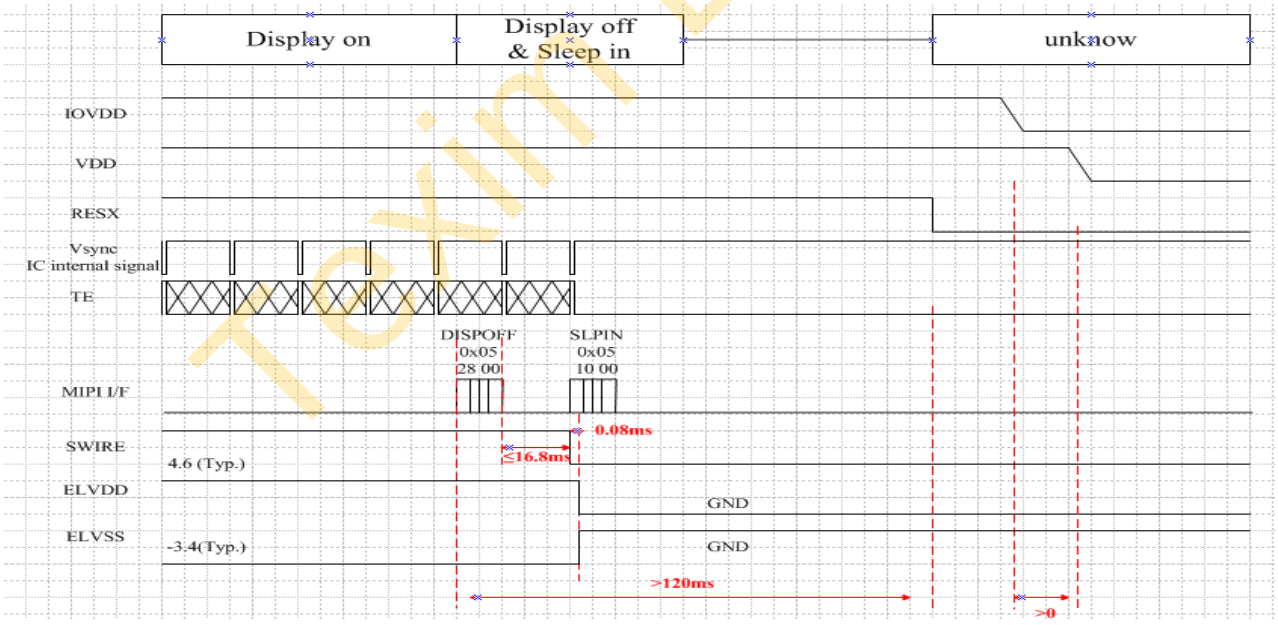
E. Recommended Operating Sequence

1. Display Power on / off Sequence

Power on sequence



Power off sequence



2. Display Initial code

Recommended Power on Initial Sequence							
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address MIPI	Data hex.	Description
1	Turn on V_{vDD}						VDD=2.8V~3.1V
2	Turn on V_{IOVDD}						IOVDD=1.8V
3	Delay	no limit					
4	REST pin low	20us					
5	REST pin high						
6	Delay	5 ms					
7			W	0x39	F0	55	
8			W			AA	
9			W			52	
10			W			08	
11			W			00	
12			W	0x39	BD	03	
13			W			20	
14			W			14	
15			W			4B	
16			W			00	
17			W	0x39	BE	03	
18			W			20	
19			W			14	
20			W			4B	
21			W			01	
22			W	0x39	BF	03	
23			W			20	
24			W			14	
25			W			4B	
26			W			00	
27			W	0x39	BB	07	
28			W			07	
29			W			07	
30			W	0x39	C7	40	
31			W	0x39	F0	55	
32			W			AA	
33			W			52	
34			W			08	
35			W			02	

36			W	0x15	EB	02	
37			W	0x39	FE	08	
38			W			50	
39			W	0x39	C3	F2	
40			W			95	
41			W			04	
42			W	0x39	E9	00	
43			W			36	
44			W			38	
45			W	0x15	CA	04	
46			W	0x39	F0	55	
47			W			AA	
48			W			52	
49			W			08	
50			W			01	
51			W	0x39	B0	03	
52			W			03	
53			W			03	
54			W	0x39	B1	05	
55			W			05	
56			W			05	
57			W	0x39	B2	01	
58			W			01	
59			W			01	
60			W	0x39	B4	07	
61			W			07	
62			W			07	
63			W	0x39	B5	03	
64			W			03	
65			W			03	
66			W	0x39	B6	55	
67			W			55	
68			W			55	
69			W	0x39	B7	36	
70			W			36	
71			W			36	
72			W	0x39	B8	23	
73			W			23	
74			W			23	

75			W	0x39	B9	03	
76			W			03	
77			W			03	
78			W	0x39	BA	03	
79			W			03	
80			W			03	
81			W	0x39	BE	32	
82			W			30	
83			W			70	
84			W	0x39	CF	FF	
85			W			D4	
86			W			95	
87			W			E8	
88			W			4F	
89			W			00	
90			W			04	
91			W	0x15	35	01	
92			W	0x15	36	00	
93			W	0x15	C0	20	
94			W	0x39	C2	17	
95			W			17	
96			W			17	
97			W			17	
98			W			17	
99			W			0B	
100	Turn on peripheral packet			0x32			Video Turn On
101			W	0x39	F0	55	
102			W			AA	
103			W			52	
104			W			08	
105			W			02	
106			W	0x39	ED	48	
107			W			00	
108			W			FF	
109			W			13	
110			W			08	
111			W			30	
112			W			0C	
113			W			00	

114	Delay	20 ms					
115	Sleep out (SLPOUT)		W	0x05	11	00	
116	Delay	300 ms					
117			W	0x39	F0	55	
118			W			AA	
119			W			52	
120			W			08	
121			W			02	
122			W	0x39	ED	48	
123			W			00	
124			W			FE	
125			W			13	
126			W			08	
127			W			30	
128			W			0C	
129			W			00	
130	Delay	20 ms					
131			W	0x39	ED	48	
132			W			00	
133			W			E6	
134			W			13	
135			W			08	
136			W			30	
137			W			0C	
138			W			00	
139	Delay	20 ms					
140			W	0x39	ED	48	
141			W			00	
142			W			E2	
143			W			13	
144			W			08	
145			W			30	
146			W			0C	
147			W			00	
148	Delay	20 ms					
149			W	0x39	ED	48	
150			W			00	
151			W			E0	
152			W			13	

153			W			08	
154			W			30	
155			W			0C	
156			W			00	
157	Delay	20 ms					
158			W	0x39	ED	48	
159			W			00	
160			W			E0	
161			W			13	
162			W			08	
163			W			00	
164			W			0C	
165			W			00	
166	Delay	20 ms					
167	Display on (DISPON)		W	0x05	29	00	
168			W	0x39	F0	55	
169			W			AA	
170			W			52	
171			W			08	
172			W			00	

Recommended Power off Mode Sequence							
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address MIPI	Data hex.	Description
1	Black pattern(黑畫面)						
2	delay	20ms					
3	Display off (DISPOFF)		W	0x05	28	00	
4	delay	20ms					
5			W	0x39	F0	55	
6			W			AA	
7			W			52	
8			W			08	
9			W			00	
10			W	0x39	C8	84	
11			W			12	
12			W			00	
13			W			00	
14			W			A0	
15			W			00	
16			W			0D	

17			W	0x39	F0	55	
18			W			AA	
19			W			52	
20			W			08	
21			W			01	
22	delay	20ms					
23			W	0x39	C2	1F	
24			W			1F	
25			W			1F	
26			W			1F	
27			W			1F	
28			W			1F	
29			W			1F	
30			W			1F	
31			W			1F	
32			W			1F	
33			W			1F	
34			W			1F	
35	delay	20ms					
36	Display on (DISPON)		W	0x05	29	00	
37	delay	20ms					
38	Display off (DISPOFF)		W	0x05	28	00	
39	Sleep in (SLPIN)		W	0x05	10	00	
40	delay	120ms					
41	REST pin low						
42	Power off						

F. Brightness Control

Recommended Power on Initial Sequence

Step	Delay time	R/W	MIPI Data Type	Address MIPI	Address Others	Data hex.	Description
1		W	0x39	F0	F000	55	
2		W			F001	AA	
3		W			F002	52	
4		W			F003	08	
5		W			F004	01	
6		W	0x39	CF	CF00	FF	CF00 control Max Brightness
7		W			CF01	D4	
8		W			CF02	95	
9		W			CF03	E8	
10		W			CF04	4F	
11		W			CF05	00	
12		W			CF06	04	

Address MIPI	Address Others	Data hex.	Gray Level
CF	CF00	00	L0
⋮	⋮		⋮
CF	CF00	80	L128
⋮	⋮	⋮	⋮
CF	CF00	FF	L255

G. Idle mode Flow

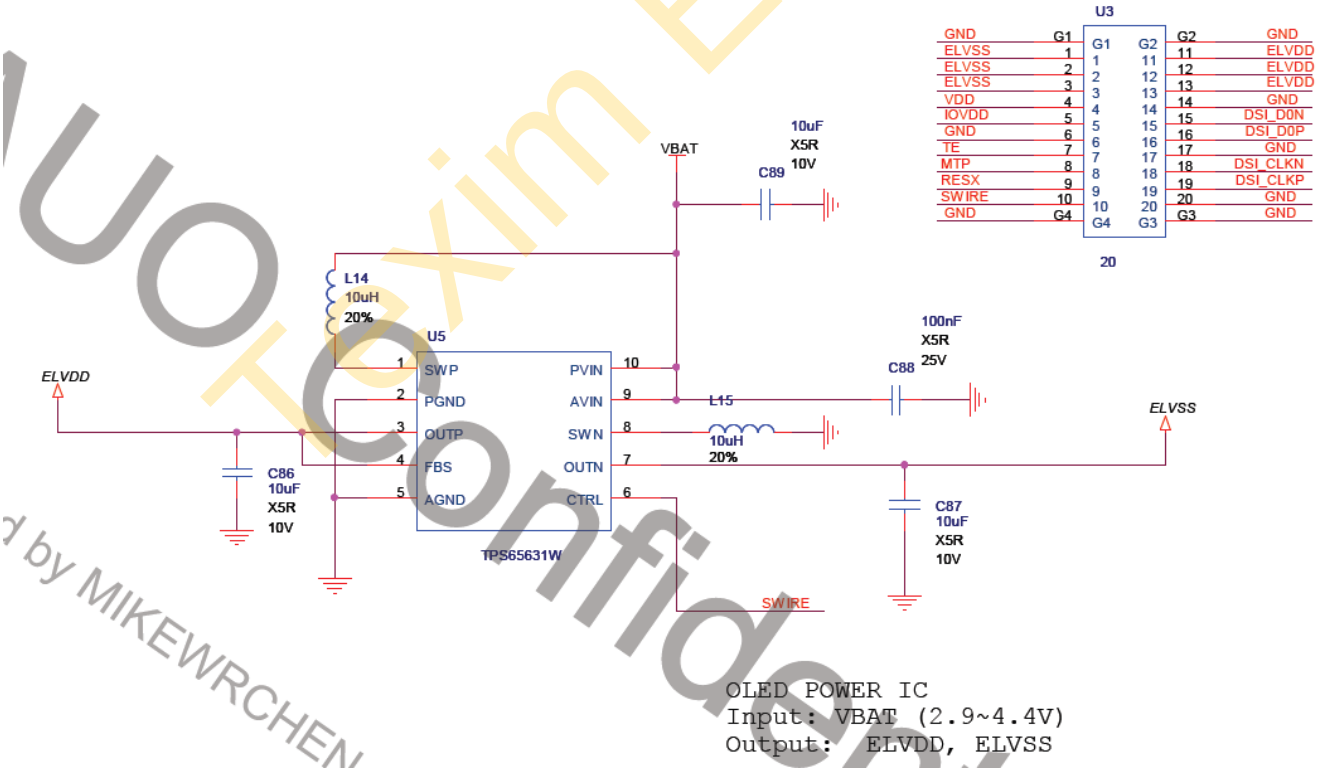
(1) Normal to Idle

Recommended Idle Initial Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Enter Idle mode		W	0x05	39	3900	00	Idle mode 30HZ

(2) Idle to Normal

Recommended Power on Initial Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Idle mode Off		W	0x05	38	3800	00	Normal mode 60HZ

H. Application Circuit



1. The 1.63" panel has to be used with power IC TPS65631W, **TI.**

   PITEK don't suggest use other power IC instead of TPS65631W, since they don't be qualified by PITEK.

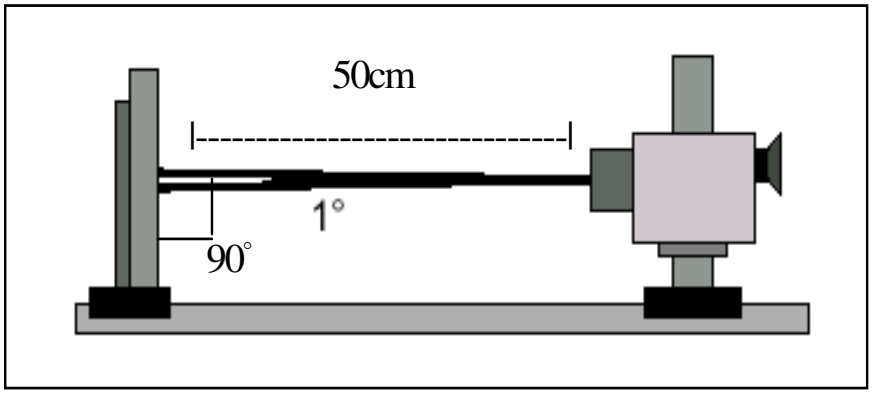
I. Specifications

Item		Abbr.	Min.	Typ.	Max.	Unit	Remark
Optical Characteristic (w/o Cover Lens)		Brightness	270	300	330	nits	Note 3
		Wx	0.275	0.305	0.335		
		Wy	0.290	0.320	0.350		
Contrast ratio		@25deg	10000	--	--		Note 4
Brightness Uniformity		300nits	75%	--	--		Note 5
Viewing angle CR>1600		Top	80°	--	--	deg	Note 6
		Bottom	80°	--	--	deg	
		Left	80°	--	--	deg	
		Right	80°	--	--	deg	
Color	Red	CIE1931 x	0.645	0.675	0.705	Red	Note 7
	Red	CIE1931 y	0.295	0.325	0.355	Red	
	Green	CIE1931 x	0.186	0.236	0.286	Green	
	Green	CIE1931 y	0.661	0.711	0.761	Green	
	Blue	CIE1931 x	0.090	0.130	0.170	Blue	
	Blue	CIE1931 y	0.025	0.065	0.105	Blue	
NTSC		CIE x , y	90	100	--	%	
Life time	T50	25℃	--	50K	--	hrs	Note 8
Crosstalk	300nits	Vertical	--	--	5.0	%	Note 9
Flicker			--	--	-30	db	Note 10
Optical Switching Time		+25℃B/W(Tr+Tf)/2	--	--	1	ms	Note 11
Gamma		γ	2.0	2.2	2.4		

Note 1: Ambient temperature =25 ℃±2 ℃

Note 2: To be measured in the dark room.

Note 3: The brightness measurement shall be done at the center of the display with a full white image. The brightness shall meet the following spec, at 100% check.

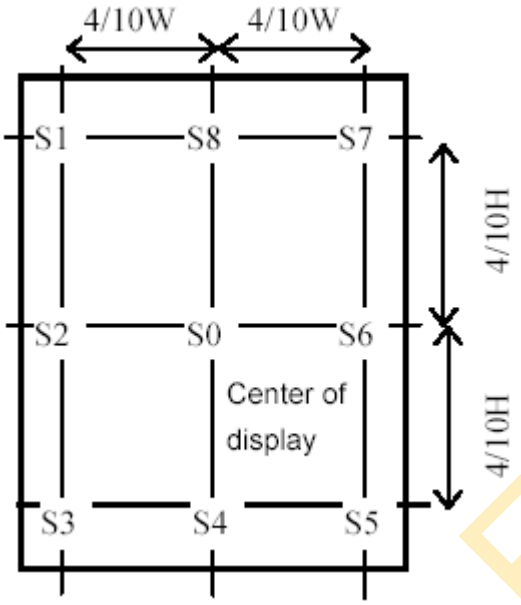


Note 4: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at “White” state}}{\text{Photo detector output when OLED is at “Black}}$$

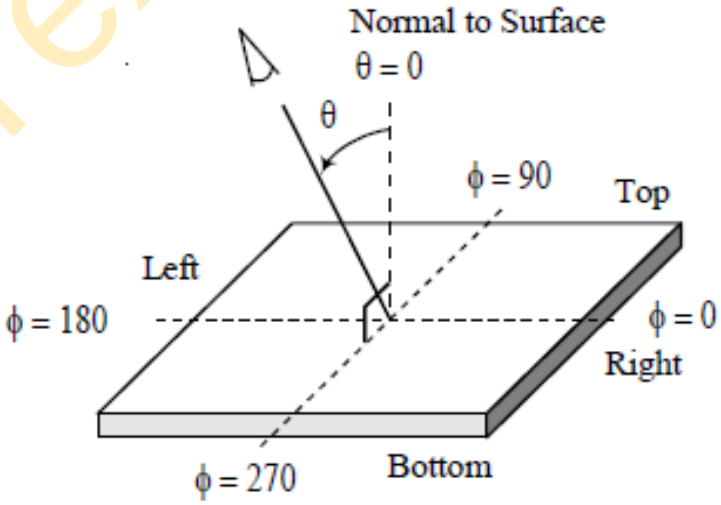
Note 5: Uniformity. Refer to figure as below



$$\text{Luminance uniformity} = \frac{\text{Minimum value from S0 to S8}}{\text{Maximum value from S0 to S8}} \times 100(\%)$$

Note 6: Definition of viewing angle :

The optical performance is specified as the driver IC located at =270°



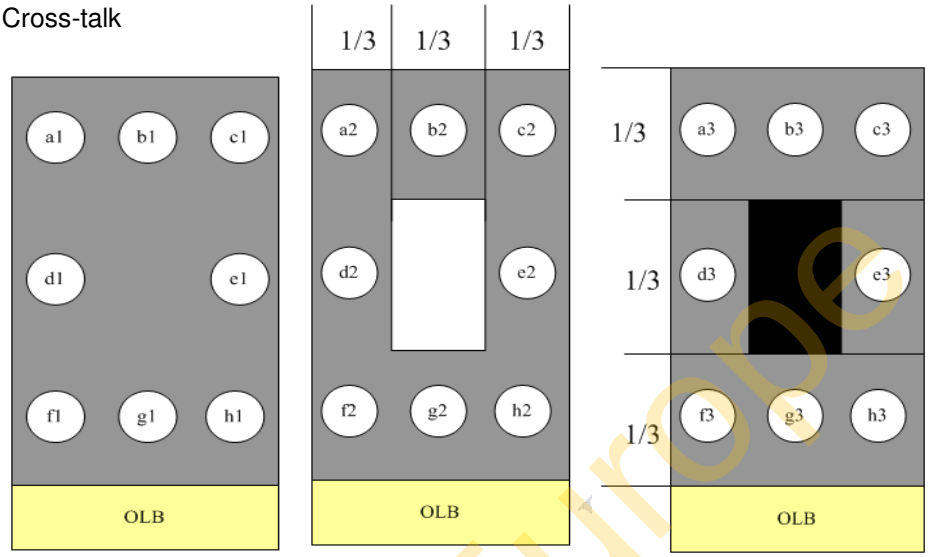
Note 7: The color chromaticity should be based on sample performance because new OLED material should be verified later.

Note 8: Time to 50% Luminance 30 Loading

Life Time (Typ) : 250 cd/m2 10K hrs , Life Time :170 cd/m2 20K hrs , Life Time :140 cd/m2 30K hrs

Life Time (Typ) : 125 cd/m2 40K hrs . Life Time :100 cd/m2 50K hrs ,

Note 9: Cross-talk



$$CrossTalk\_White = \begin{cases} 1-\left(\frac{b2}{a2}\div\frac{b1}{a1}\right)\times 100\%, 1-\left(\frac{b2}{c2}\div\frac{b1}{c1}\right)\times 100\%, \\ 1-\left(\frac{d2}{a2}\div\frac{d1}{a1}\right)\times 100\%, 1-\left(\frac{d2}{f2}\div\frac{d1}{f1}\right)\times 100\%, \\ 1-\left(\frac{e2}{c2}\div\frac{e1}{c1}\right)\times 100\%, 1-\left(\frac{e2}{h2}\div\frac{e1}{h1}\right)\times 100\%, \\ 1-\left(\frac{g2}{f2}\div\frac{g1}{f1}\right)\times 100\%, 1-\left(\frac{g2}{h2}\div\frac{g1}{h1}\right)\times 100\% \end{cases}$$

$$CrossTalk\_Black = \begin{cases} 1-\left(\frac{b3}{a3}\div\frac{b1}{a1}\right)\times 100\%, 1-\left(\frac{b3}{c3}\div\frac{b1}{c1}\right)\times 100\%, \\ 1-\left(\frac{d3}{a3}\div\frac{d1}{a1}\right)\times 100\%, 1-\left(\frac{d3}{f3}\div\frac{d1}{f1}\right)\times 100\%, \\ 1-\left(\frac{e3}{c3}\div\frac{e1}{e1}\right)\times 100\%, 1-\left(\frac{e3}{h3}\div\frac{e1}{h1}\right)\times 100\%, \\ 1-\left(\frac{g3}{f3}\div\frac{g1}{f1}\right)\times 100\%, 1-\left(\frac{g3}{h3}\div\frac{g1}{h1}\right)\times 100\% \end{cases}$$

$$CrossTalk = MAX\{CrossTalk\_White, CrossTalk\_Black\}$$

Note 10: Flicker

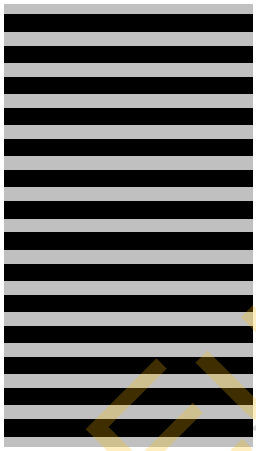
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

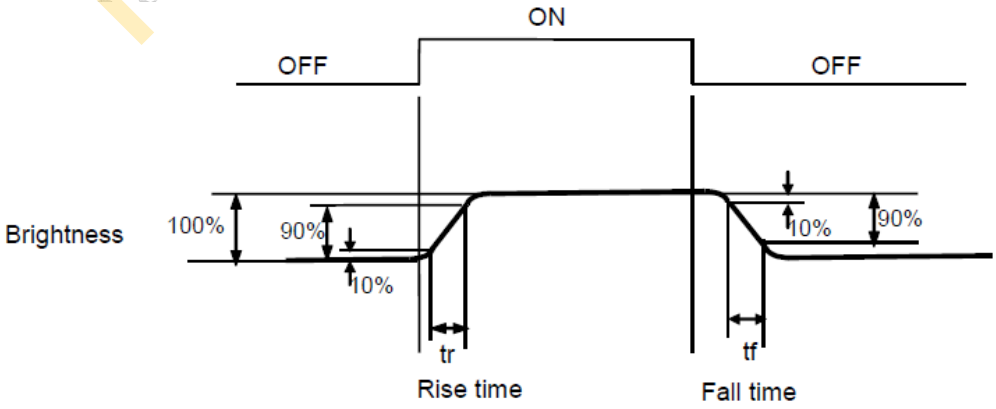
The flicker level shall be measured with the test pattern in below.

The gray leves of test pattern is 128.



Note 11: Optical Switching Time:

The optical switching time measurements should be performed at driven BLACK and driven WHITE at typ. brightness setting by the driving techniques specified. The luminance should be measured with the emitting display and the detector at θ=0°and ψ=90°. The rise time tr is the time between a 10% optically response of the display and a 90% optically response of the display. The fall time tf is the time between a 10% optically response of the display and a 90% optically response to the display. The response time is defined as the average of the rise time and the fall time.

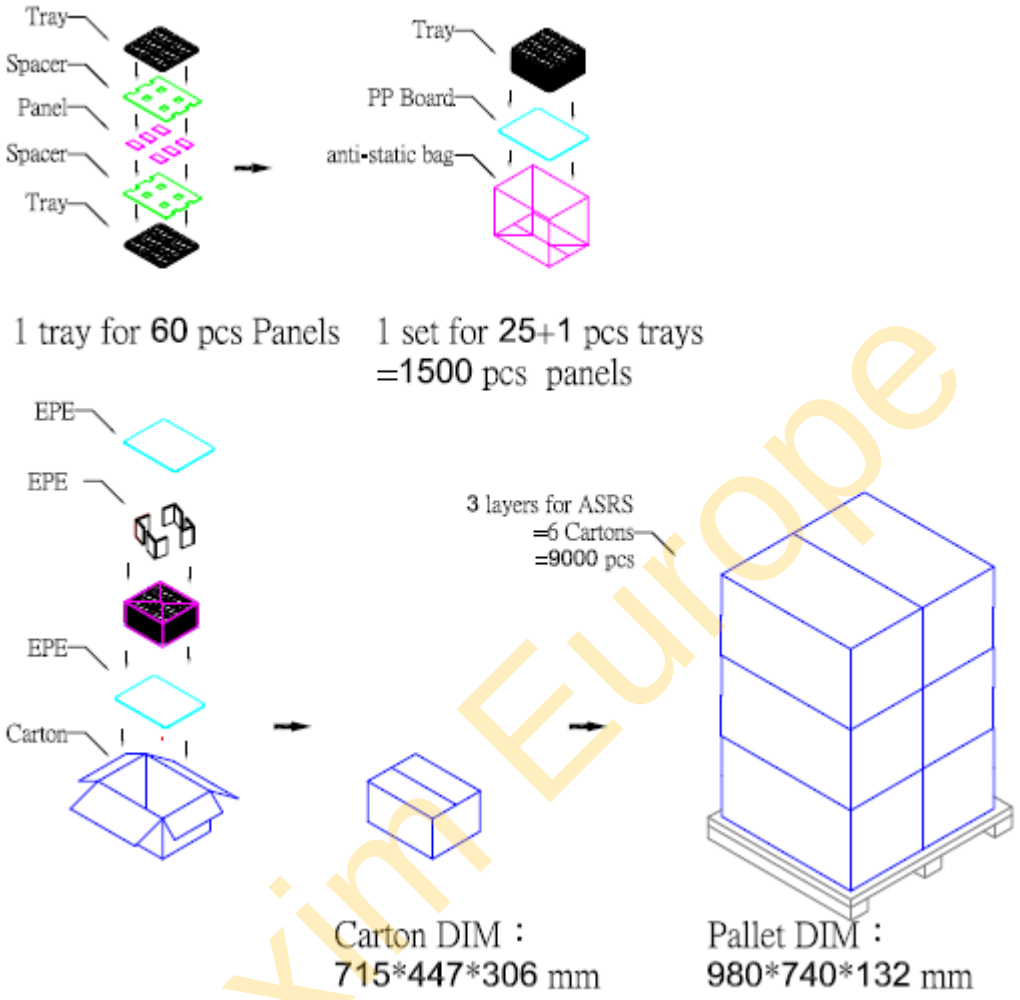


J. Reliability Test Items

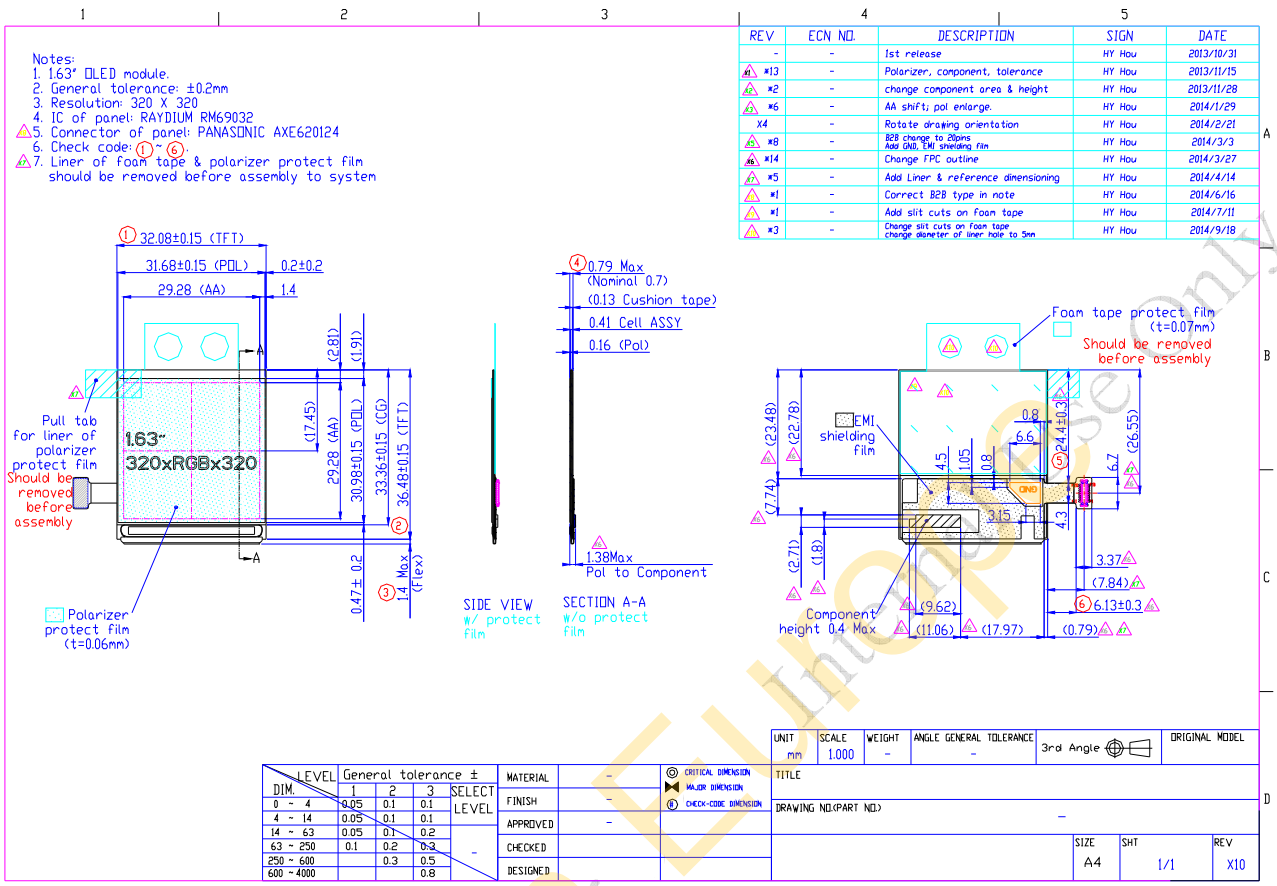
Category	No.	Test items	Conditions	Remark
Reliability (Environment)	1	High Temp. Operation	Ta= 60ºC 168hrs	Ta: Ambient temperature.
	2	High Temp. Storage	Ta= 70 ºC 168hrs	Non-operation
	3	Low Temp. Operation	Ta= -20 ºC 168hrs	
	4	Low Temp. Storage	Ta= -30 ºC 168hrs	Non-operation
	5	High Temp./Humi. Operation	Ta= 40 ºC. 95% RH 168hrs	
	6	Thermal Shock	-30 ºC ~70 ºC, Dwell for 30 min. 30 cycles.	Non-operation
	7	Vibration test	Random 1.5G,10~200Hz,30min/axis	Non-operation

Judge Criteria:No functional defect

K. Packing



L. Outline Demension



M. Precaution:

Please pay attention to the following items when you use the OLED Modules(Panel):

7-1 Do not twist or bend the module(panel) and prevent the unsuitable external force for display during assembly.
7-2 Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.
7-3 Avoid dust or oil mist during assembly.
7-4 Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module(panel).
7-5 Less EMI: it will be more safety and less noise.
7-6 Please operate module(panel) in suitable temperature. The response time & brightness will drift by different temperature.
7-7 Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
7-8 Please be sure to turn-off the power when connecting or disconnecting the circuit.
7-9 Polarizer scratches easily, please handle it carefully.
7-10 Display surface never likes dirt or stains.
7-11 A dew drop may lead to destruction. Please wipe off any moisture before using module(panel).
7-12 Sudden temperature changes cause condensation, and it will cause polarizer damaged.
7-13 High temperature and humidity may degrade performance. Please do not expose the module(panel) to the direct sunlight and so on.
7-14 Acetic acid or chlorine compounds are not friends with AMOLED display module(panel).
7-15 Static electricity will damage the module(panel), please do not touch the module(panel) without any grounded device.
7-16 Please avoid any static electricity damage (ESD) during producing and operating.
7-17 Do not disassemble and reassemble the module(panel) by self.
7-18 Be careful do not touch the rear side directly.
7-19 No strong vibration or shock. It will cause module(panel) broken.
7-20 Storage the modules(panel) in suitable environment with regular packing.
7-21 Be careful of injury from a broken display module(panel).
7-22 Please avoid the pressure adding to the surface (front or rear side) of modules(panel), because it will cause the display non-uniformity or other function issue.