MATRIX ORBITAL

EVE2 TFT Module

Hardware Manual

Revision 1.2

Revision History

Revision	Date	Description	Author
1.2	October 23rd, 2017	Corrected bezel information in section 2.1. Added additional header information	Divino
1.1	October 10th, 2017	Added link to FTDI Programmers Guide	Divino
1.0	August 3rd, 2017	Initial Release	Divino

Contents

1 Introduction

The Matrix Orbital EVE lineup utilizes FTDI's second generation Embedded Video Engine to control, render, manage and display complex graphics on a full color TFT touch screen. By taking advantage of the 1 megabyte of graphics RAM, motion-JPEG encoded AVI videos can be played back in both portrait and landscape mode. Data can be displayed through a set of widgets such as gauges, spinners, sliders, and bar graphs.

Additional features include added touch control hardware, capable of recognizing and tracking touch movement and providing notification for up to 255 touch objects. Mono 8-bit linear audio wave playback at sampling frequencies from 8 kHz to 48 kHz is made possible by the built-in sound synthesizer and digital filter.

The EVE 2 communicates using SPI protocol, and can be configured for quad SPI communication. Using SPI communication protocol makes the EVE 2 compatible with many microcontrollers available on the market, including the FTDI FT900, NXP 17XX, Arduino, and many more. With built-in graphics operations, and support for multiple widgets, development of high-quality user interface screens is simplified.

1.1 Key Features

- Advanced Embedded Video Engine(EVE) with high resolution graphics and video playback
- Support multiple widgets for simplified design development
- Support for Resistive and Capacitive Touch Screen Technology
- Support capacitive touch screen with up to 5 touches detection
- Support for LCD display with resolution up to SVGA (800x600) and formats with data enable (DE) mode or VSYNC/HSYNC mode
- Support landscape and portrait orientations
- Support playback of motion-JPEG encoded AVI videos
- -20°C to 70°C extended operating temperature range

1.2 Block Diagram

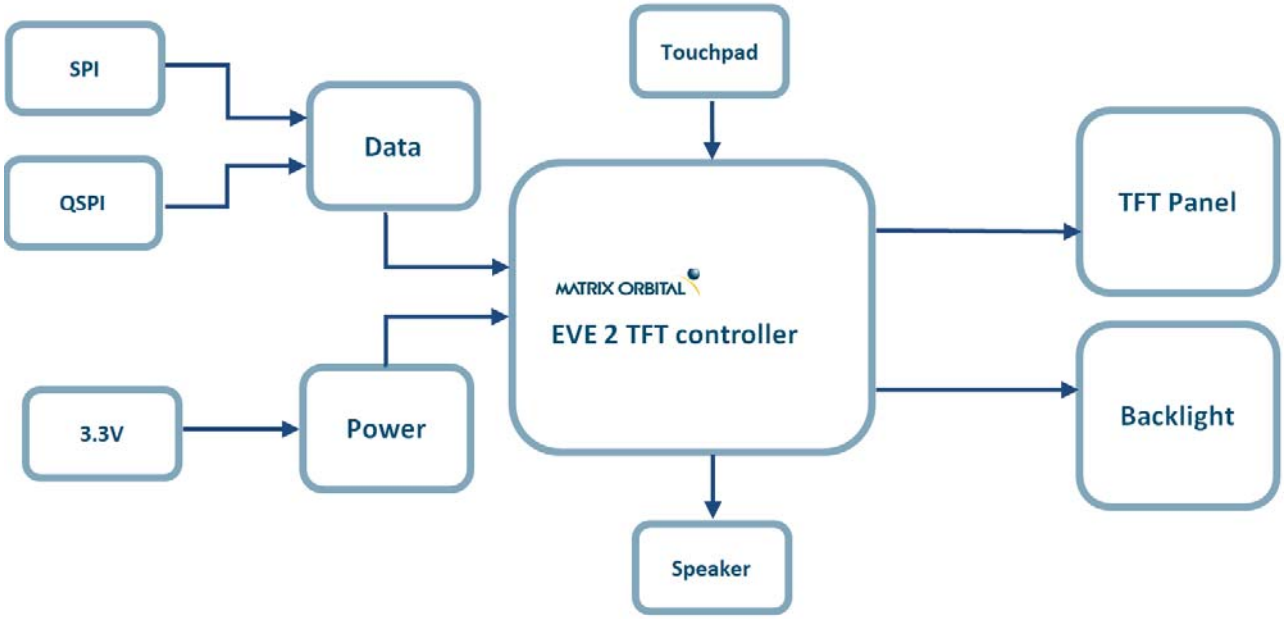

Figure 1: EVE2 TFT Module Block Diagram

2 FTDI EVE Chip

FTDI Chip develops innovative silicon solutions that enhance interaction with the latest in global technology. The major objective from the company is to 'bridge technologies' in order to support engineers with highly sophisticated, feature-rich, robust and simple-to-use product platforms. These platforms enable creation of electronic designs with high performance, low peripheral component requirements, low power budgets and minimal board real estate.

2.1 FTDI EVE Graphics Engine

The FT81X series chips are graphics controllers with add-on features such as audio playback and touch capabilities. They consist of a rich set of graphics objects (primitive and widgets) that can be used for displaying various menus and screen shots for a range of products including home appliances, toys, industrial machinery, home automation, elevators, and many more.

EVE graphics controller ICs combine display, touch and audio functionality within a single chip and take an innovative object-oriented approach to HMI implementation that is proving highly effective. It leads to more streamlined solutions that are simpler to create, with significantly lower component counts, reduced board space requirements, curbed power consumption, etc. The second generation EVE devices at the heart of these new development modules have greater pixel resolution than the previous EVE ICs, resulting in sharper image rendering and greater colour depth. They also have accelerated data transfer and image/video loading capabilities, enhanced video playback, plus expanded memory resources.

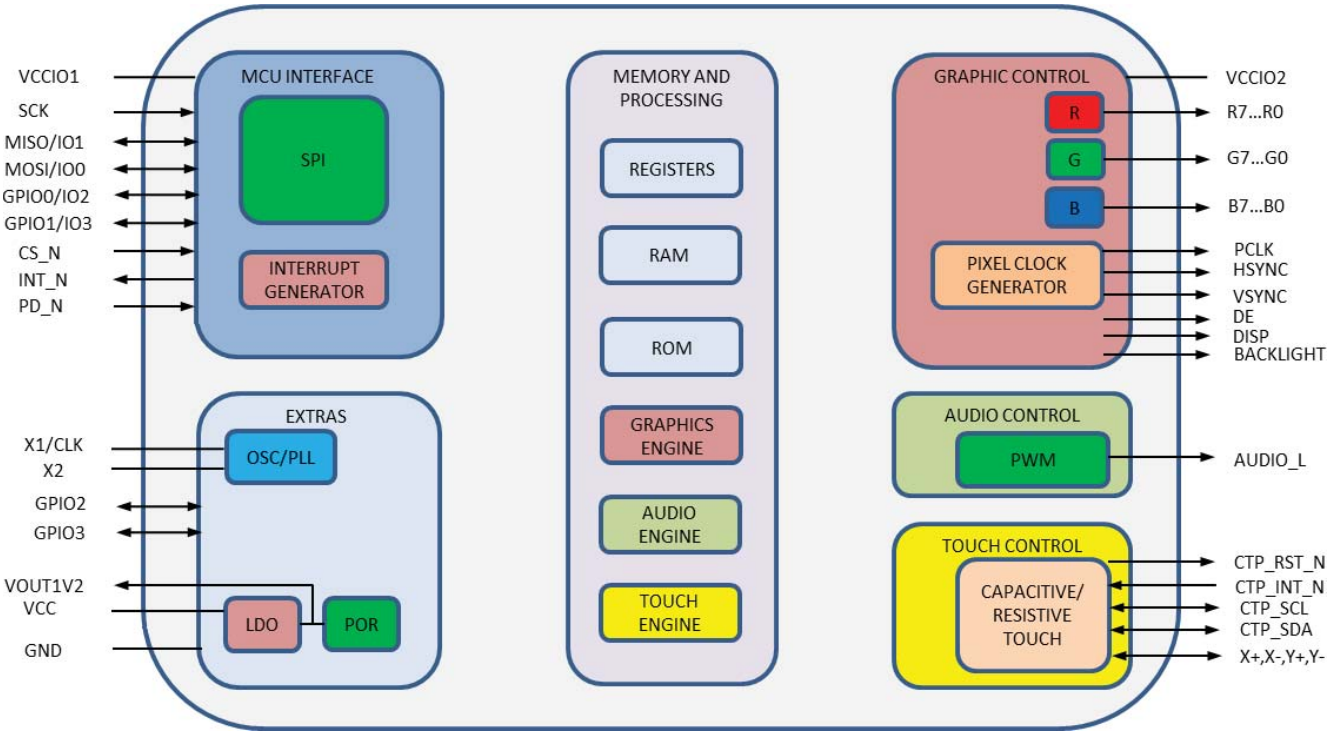

Figure 2: EVE 2 Embedded Video Engine

More details regarding the EVE2 hardware specs can be found in the FTDI FT81x Datasheet, available online.
An FTDI EVE2 programming guide, titled "FT81x Series Programming Guide", is also available and can be downloaded at FTDI/Bridgetek's website http://www.brtchip.com/ft81x

3 EVE2 Headers

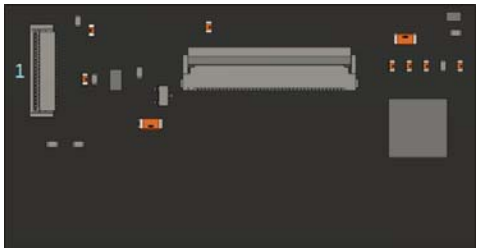

Figure 3: EVE2 Module Header Locations

Table 1: List of available Headers

#	Header	Standard Mate
1	SPI Communication and Power	FFC-20P

3.1 Communication Header Pinout

The 20 pin FFC header on the EVE2 TFT Module is used to interface with an SPI controller, and is compatible with a number of 20 pin ribbon cables. Any 20 pin FFC cable with a 0.5mm pitch and bottom contacts, such as the Wurth Electronics INC 687620050002 series ribbon cable will be compatible with the EVE2 module.

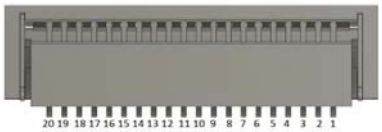

Figure 4: 20 pin FFC communication header

Table 2: 20 pin FFC communication header pinout

Pin	Symbol	Type	Function
1	VCC	Power	Logic Voltage (3.3V)
2	GND	Ground	Ground Connection
3	SCK	Input	SPI clock input
4	MISO	Input/output	SPI Single mode: SPI MISO output SPI Dual/Quad mode: SPI data line 1
5	MOSI	Input/output	SPI Single mode: SPI MISO input SPI Dual/Quad mode: SPI data line 0
6	CS	Input	SPI slave select input.*
7	$\overline{\text{INT}}$	Open Drain Output	Interrupt to host**
8	RST		FT81x Reset pin
9	N/C	No connection	No connection
10	AUDIO	Output	Audio PWM out
11	IO2	Input/output	SPI Single/Dual mode: General purpose IO 0 SPI Quad mode: SPI data line 2
12	IO3	Input/output	SPI Single/Dual mode: General purpose IO 1 SPI Quad mode: SPI data line 3
13	GPIO2	Input/output	General purpose IO 2
14	GPIO3	Input/output	General purpose IO 3
15	GND	Ground	Ground connection
16	VCC	Power	Logic Voltage (3.3V)
17	BLVDD	VDD	Backlight Voltage
18	BLVDD	VDD	Backlight Voltage
19	BLGND	Ground	Backlight Ground
20	BLGND	Ground	Backlight Ground

***Note:** The CS pin signifies when a SPI transaction occurs by going active low. When the pin goes inactive high, the write operation is considered complete.

****Note:** Open drain output (default) or push-pull output, active low

4 Communication Model

4.1 Programming Model

The FT81X appears to the host MCU as a memory-mapped SPI device. The host MCU sends commands and data over the serial protocol described in the data sheet.

4.2 General Software Architecture

The software architecture can be broadly classified into layers such as custom applications, graphics/GUI manager, video manger, audio manager, drivers etc. FT81X higher level graphics engine commands and co-processor engine widget commands are part of the graphics/GUI manager. Control & data paths of video and audio are part of video manager and audio manager. Communication between graphics/GUI manager and the hardware is via the SPI driver. Typically the display screen shot is constructed by the custom application based on the framework exposed by the graphics/GUI manager.

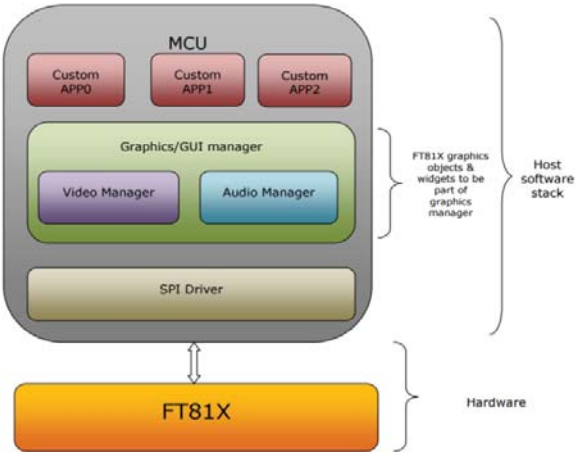

Figure 5: EVE 2 Programmer model

5 Communication Interface

5.1 SPI Interface Timing Specification

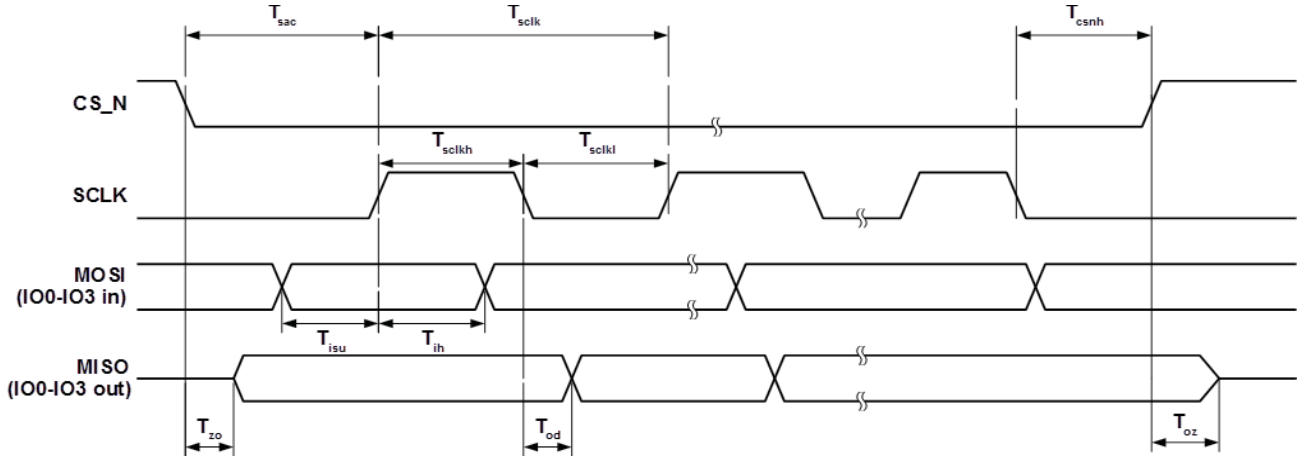

Figure 6: SPI Timing Diagram

Table 3: SPI Timing Signals

Parameter	Description	VCCIO = 3.3V		Units
		Min	Max	
Tsclk	SPI Clock Period (SINGLE/DUAL mode)	33.3		ns
Tslck	SPI clock Period (QUAD mode)	40		ns
Tsclkl	SPI clock low duration	13		ns
Tsclkh	SPI clock high duration	13		ns
Tsac	SPI access time	3		ns
Tisu	Input Setup	3		ns
Tih	Input hold	0		ns
Tzo	Output enable delay		11	ns
Toz	Output disable delay		10	ns
Tod	Output data delay		11	ns
Tcsnh	CSN hold time	0		ns

5.2 SPI and QSPI communication

The EVE2 TFT Module is capable of communicating to hosts and microcontrollers through a quad serial parallel interface (QSPI). Only SPI mode 0 is supported. The QSPI slave interface can operate up to 30MHZ, and can be configured in SINGLE, DUAL or QUAD channel modes.

The SPI slave defaults to SINGLE channel mode operation, using MISO as output to the master and MOSI as input from the master. The SPI slave can be configured to allow DUAL and QUAD channel modes by writing to register REG_SPI_WIDTH while in single channel mode.

Table 4: SPI/QSPI Communication Configuration

REG_SPI_WIDTH[1:0]	Channel Mode	Data pins	Max bus speed
00	SINGLE - default mode	MISO, MOSI	30 MHz
01	DUAL	IO0, IO1	30 MHz
10	QUAD	IO0, IO1, IO2, IO3	25 MHz
11	Reserved	-	-

When DUAL/QUAD channel modes are enabled, the SPI data ports become unidirectional. SPI transactions will be signified by CS going active low when DUAL/QUAD modes are active, and data ports are set as inputs.

Hence, for writing to the FT81x, the protocol is “WR-Command/Addr2, Addr1, Addr0, DataX, DataY, DataZ …” The write operation is considered complete when CS goes inactive high.

For reading from the FT81x, the protocol is “RD-Command/Addr2, Addr1, Addr0, Dummy-Byte, DataX, DataY, DataZ”. However as the data ports are now unidirectional, a change of port direction will occur before DataX is clocked out of the FT81x. Therefore it is important that the firmware controlling the SPI master changes the SPI master data port direction to “input” after transmitting Addr0. The FT81x will not change the port direction till it starts to clock out DataX. Hence, the Dummy-Byte cycles will be used as a change-over period when neither the SPI master nor slave will be driving the bus; the data paths thus must have pull-ups/pull-downs. The SPI slave from the FT81x will reset all its data ports’ direction to input once CS goes inactive high (i.e. at the end of the current SPI master transaction).

The below diagram depicts the behaviour of both the SPI master and slave in the master read case.

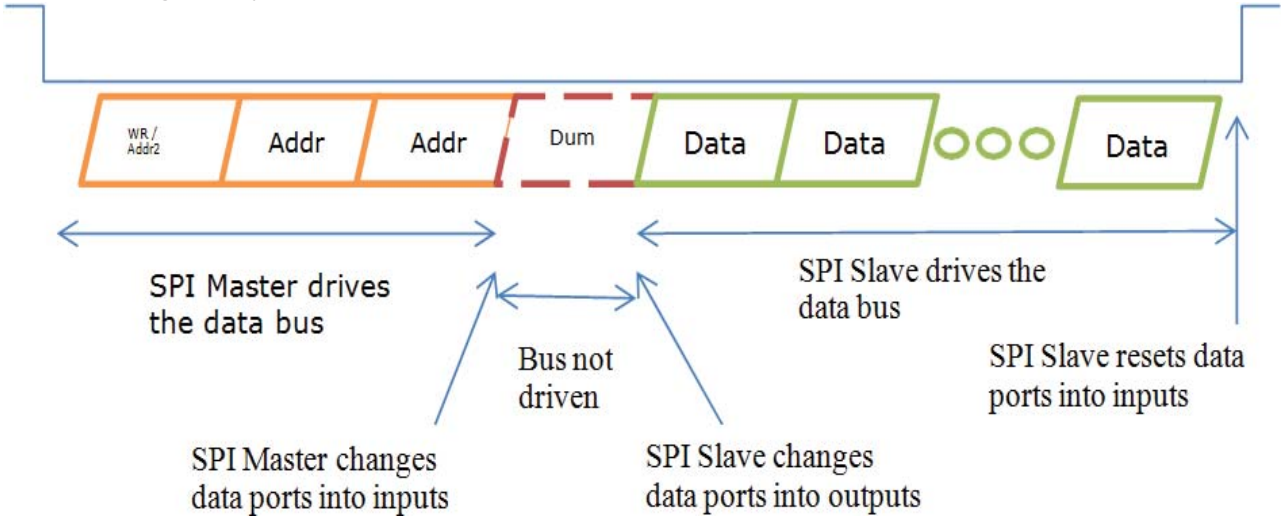

Figure 7: SPI Master and Slave bus behaviour

For DUAL channel operation, MISO(MSB) and MOSI are used. In Quad channel operation, IO3(MSB), IO2, MISO, and MOSI are used.

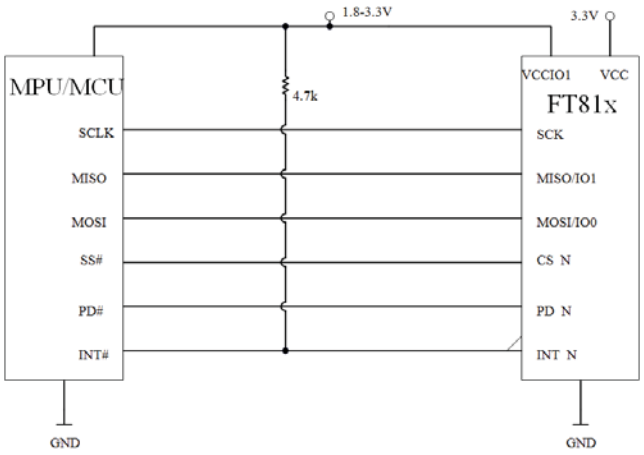

Figure 8: Single/Dual Channel SPI Interface connection

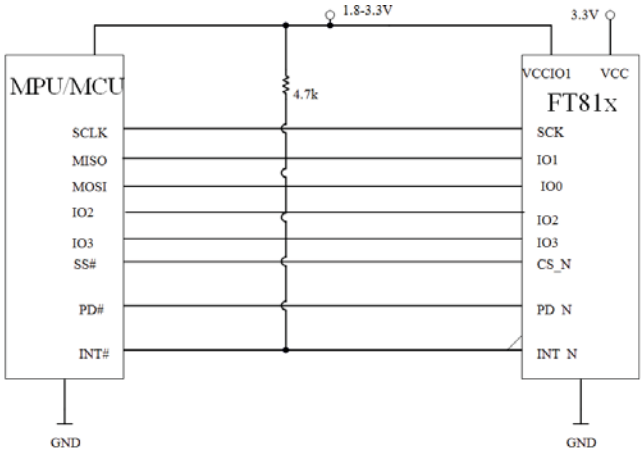

Figure 9: Quad channel SPI Interface connection

5.3 Serial Data Protocol

When interfaced with a host, the FT81x will appear as a memory-mapped SPI device. Communication between the host and the FT81x is accomplished through a series of reads and writes to a large (4 megabyte) address space. Within this address space are dedicated areas for graphics, audio and touch control.

The FT81x address space is read and written to using SPI transactions. Memory read, memory write and command write transactions are sent by the most significant bit first.

Each transaction starts with CS going low, and ends when CS going high. Data transactions have no limit regarding data length, so long as the memory address is continuous.

When initiating an SPI memory read transaction, the host will send two zero bits, followed by the 22-bit address. A dummy byte follows the address, and the FT81x will respond to each host byte with read data bytes.

Table 5: SPI Memory read transaction

7	6	5	4	3	2	1	0	
0	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Dummy byte								
Byte 0								Read Address
Byte n								

For SPI memory write transactions, a ‘1’ bit and ‘0’ bit is sent by the host, followed by the 22-bit address. The write data follows.

Table 6: SPI Memory write transaction

7	6	5	4	3	2	1	0	
1	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Dummy byte								
Byte 0								Read Address
Byte n								

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 7: EVE2 Module Limiting Values

Item	Value	Unit
Storage Temperature	-30 to 80	°C
Ambient Temperature (Power Applied)	-20 to +70	°C
VCC Supply Voltage	0 to +4	V
DC Input Voltage	-0.5 to + (VCCIO + 0.3)	V

6.2 DC Characteristics

Table 8: EVE2 DC characteristics

Item	Description	Min.	Typ.	Max.	Unit	Conditions
VCC	VCC operating supply voltage	2.97	3.30	3.63	V	Normal Operation
Icc1	Power Down Current	-	0.17	-	mA	Power down mode
Icc2	Sleep Current	-	0.76	-	mA	Sleep Mode
Icc3	Standby Current	-	1.8	-	mA	Standby Mode
Icc4	Operating Current	-	22	-	mA	Normal Operations

6.3 Digital I/O Pin Characteristics

Table 9: Digital I/O Specifications

Parameter	Description	Min	Typ.	Max	Units	Conditions
Voh	Output Voltage High	VCCIO- 0.4	3.3V-	-	V	Ioh=5mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=5mA
Vih	Input High Voltage	2.0	-	-	V	
Vil	Input Low Voltage	-	-	0.8	V	
Vth	Schmitt Hysteresis Voltage	0.22	-	0.3	V	
Iin	Input leakage current	-10	-	10	uA	Vin = VCCIO or 0
Ioz	Tri-state output leakage current	-10	-	10	uA	Vin = VCCIO or 0
Rpu	Pull-up resistor	-	42	-	kΩ	
Rpd	Pull-down resistor	-	44	-	kΩ	

6.4 Touch Sense Characteristics

Table 10: Touch Panel characteristics

Parameter	Description	Min	Typ.	Max	Units	Conditions
Rsw-on	X-,X+,Y- and Y+ Drive On resistance	-	6	10	Ω	VCCIO=3.3V
Rsw-off	X-,X+,Y- and Y+ Drive Off resistance	10	-	-	MΩ	
Rpu	Touch sense pull up resistance	78	100	125	kΩ	
Vth+	Touch Detection rising-edge threshold on XP pin	1.59	-	2.04	V	VCCIO=3.3V
Vth-	Touch Detection falling-edge threshold on XP pin	1.23	-	1.55	V	VCCIO=3.3V
Rl	X-axis and Y-axis drive load resistance	200	-	-	Ω	

7 Ordering Options

7.1 Matrix Orbital Eve 2 series displays

The EVE2 TFT Module has multiple size and touch variants, to ensure that there is an option for every application. Resistive touch panels are also available, allowing interactive touch functionality for all applications.

Table 11: EVE2 Displays, and GTT counterpart

Size	Touch Screen Type	Matrix Orbital Part Number	Intelligent Series Upgrade
2.9”	None	EVE2-29A-BLM-TPN	GTT29A-TPN-BLM-B0-H1
3.5”	None	EVE2-38A-BLH-TPR	GTT35A TPN-BLM-B0-H1
	Resistive	EVE2-35A-BLM-TPN	GTT35A TPR-BLM-B0-H1
3.8”	None	EVE2-35A-BLM-TPR	GTT38A-TPR-BLH-B0-H1
4.3”	None	EVE2-43A-BLM-TPN	GTT43A TPN-BLM-B0-H1
	Resistive	EVE2-43A-BLM-TPR	GTT43A TPR-BLM-B0-H1
5.0”	None	EVE2-50A-BLM-TPN	GTT50A TPN-BLM-B0-H1
	Resistive	EVE2-50A-BLM-TPR	GTT50A TPR-BLM-B0-H1
7.0”	None	EVE2-70A-BLM-TPN	GTT70A TPN-BLM-B0-H1
	Resistive	EVE2-70A-BLM-TPR	GTT70A TPR-BLM-B0-H1

7.2 Matrix Orbital Product Line Comparison

Table 12: Product comparison chart

Features		Display Series		
		Parallel	EVE2	GTT
Memory	Storage			2GB
	RAM		1MB	32/64MB
Interface	RS232			✓
	TTL			✓
	I2C			✓
	RS422			✓
	USB			✓
	Parallel	✓		
	SPI		✓	
Touch	None	✓	✓	✓
	Resistive	✓	✓	✓
	PCAP	✓	✓	✓
	Keyboard			✓
Features	Piezo			✓
	Vibration feedback			✓
	Audio playback		✓	
	GPO		4	10
Voltage	3.3V		✓	
	5V	✓		✓
	9-35V			✓
Development Time		•••••	•••	•
Cost		$	$$	$$$$

7.3 Software Support

Table 13: EVE Screen Editor and GTT Designer Suite comparison

Features	FTDI EVE Screen Editor	GTT Designer Suite
Drag and drop functionality	✓	✓
Send commands directly to display	✓	✓
Command list generation	✓	✓
Intuitive design format	✓	✓
Deploy screens to the display	-	✓
Multiple screen generation	-	✓
Device Inspector	✓	-

7.4 EVE2 Module Displays

The EVE2 Module is paired with a Matrix Orbital Parallel TFT display. Information about Matrix Orbital's Parallel TFT lineup, including drawings, dimensions, and tolerances can be found online at:

https://www.matrixorbital.ca/manuals/parallel-display/mop-tft-manual

8 Dimensional Drawing

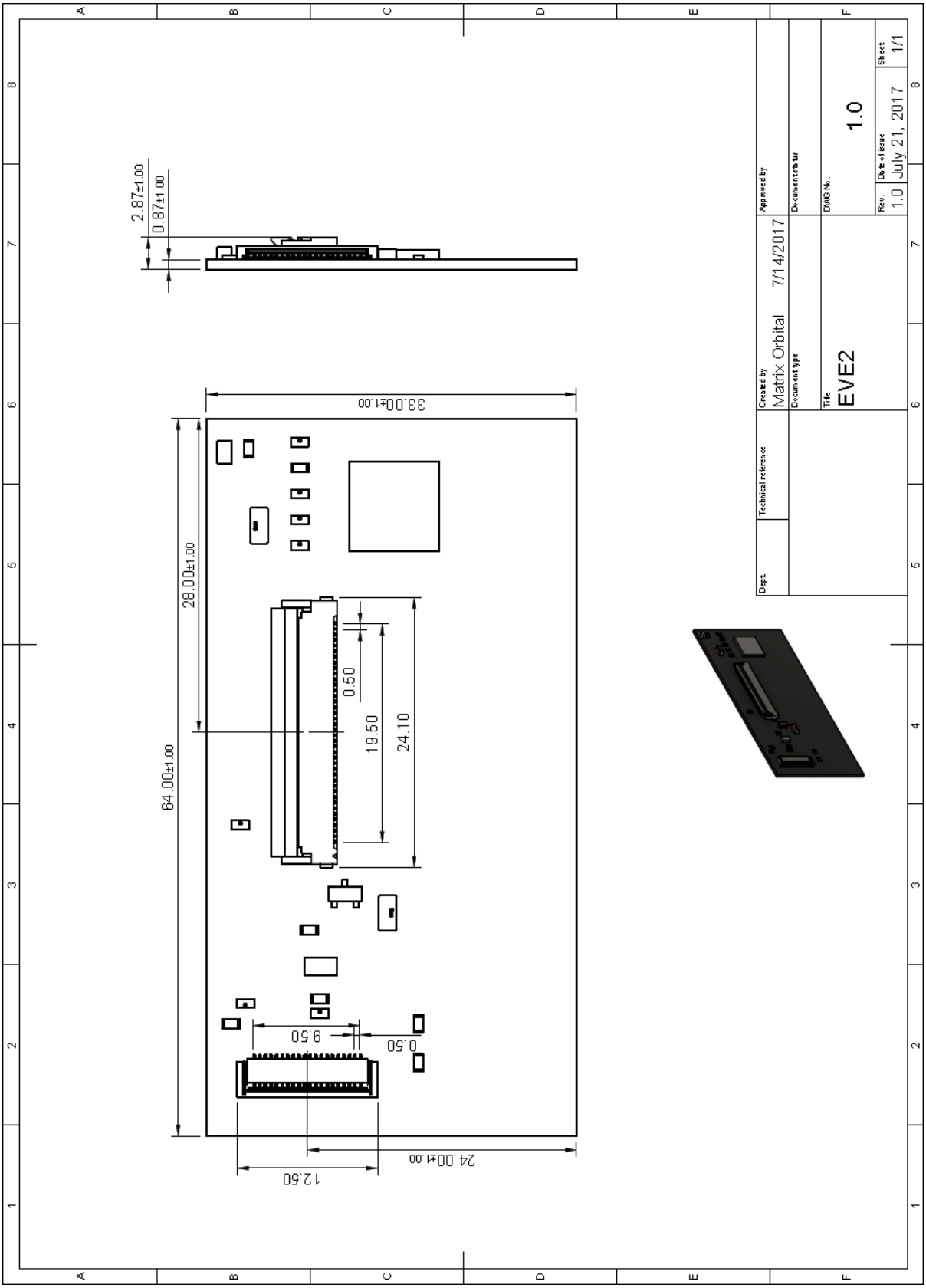

Figure 10: EVE2 TFT Module Technical Drawing

9 EVE2 TFT Module Schematic

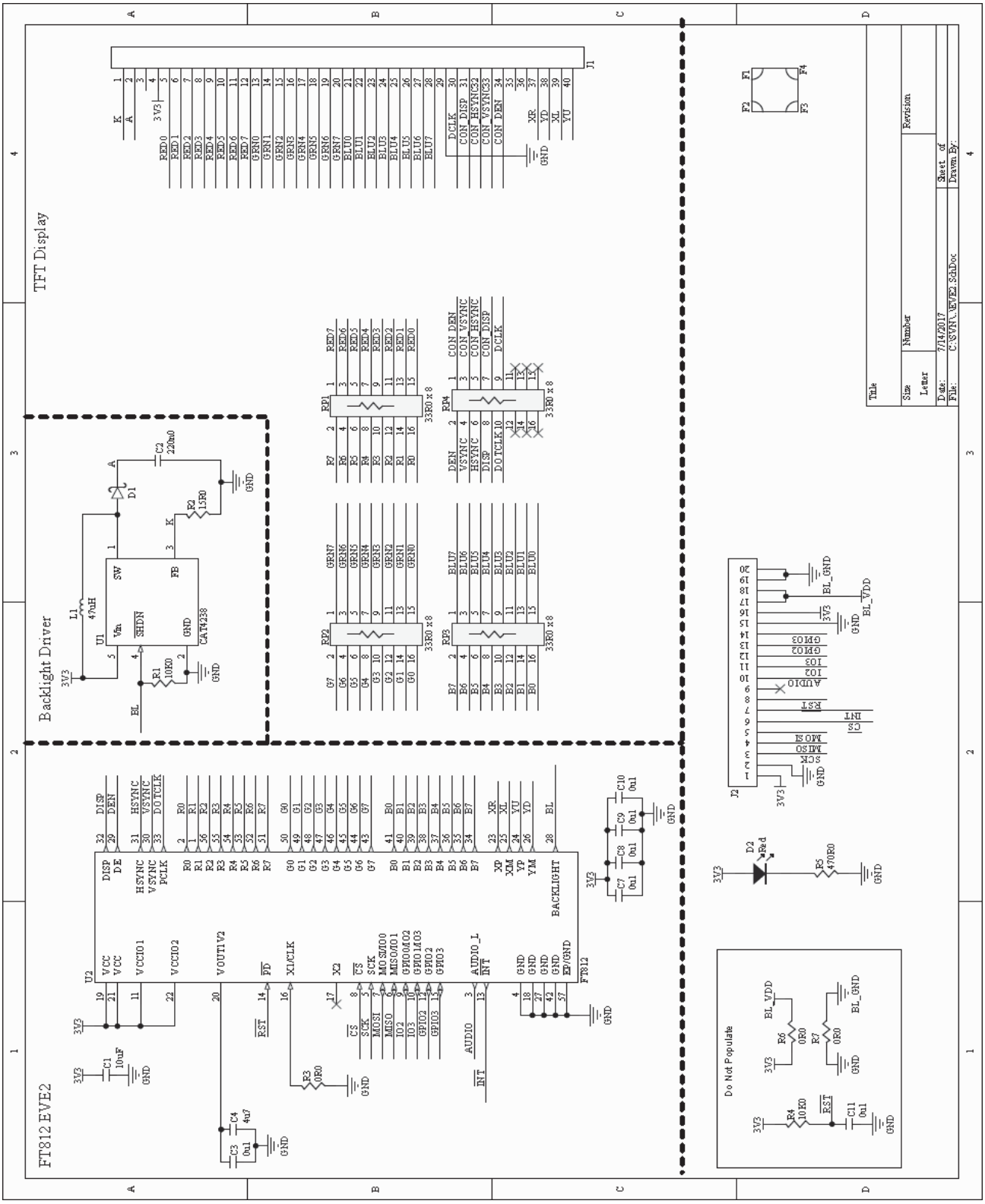

Figure 11: EVE2 TFT Module Schematic

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