TFT DISPLAY SPECIFICATION

WINSTAR Display Co.,Ltd.
華凌光電股份有限公司

Winstar Display Co., LTD
華凌光電股份有限公司
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SPECIFICATION

CUSTOMER : _____

MODULE NO.: WF35XSWACDNN0#

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
			葉虹蘭
ISSUED DATE: 2021/07/30			

TFT Display Inspection Specification: https://www.winstar.com.tw/technology/download.html
Precaution in use of TFT module: https://www.winstar.com.tw/technology/download/declaration.html

Winstar Display Co., LTD
華凌光電股份有限公司

MODLE NO：

RECORDS OF REVISION

DOC. FIRST ISSUE

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2021/07/30		First issue

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1.Module Classification Information

W	F	35	X	S	W	A	C	D	N	N	0	#
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

①	Brand：WINSTAR DISPLAY CORPORATION		
②	Display Type：F→TFT Type, J→Custom TFT		
③	Display Size：3.5” TFT		
④	Model serials no.		
⑤	Backlight Type：	F→CCFL, White S→LED, High Light White	T→LED, White Z→Nichia LED, White
⑥	LCD Polarize Type/ Temperature range/ Gray Scale Inversion Direction	A→Transmissive, N.T, IPS TFT C→Transmissive, N. T, 6:00 ; F→Transmissive, N.T,12:00 ; I→Transmissive, W. T, 6:00 K→Transflective, W.T,12:00 L→Transmissive, W.T,12:00 N→Transmissive, Super W.T, 6:00	Q→Transmissive, Super W.T, 12:00 R→Transmissive, Super W.T, O-TFT V→Transmissive, Super W.T, VA TFT W→Transmissive, Super W.T, IPS TFT X→Transmissive, W.T, VA TFT Y→Transmissive, W.T, IPS TFT Z→Transmissive, W.T, O-TFT
⑦	A：TFT LCD B：TFT+SCREW HOLES+CONTROL BOARD C：TFT+ SCREW HOLES +A/D BOARD D：TFT+ SCREW HOLES +A/D BOARD+CONTROL BOARD E：TFT+ SCREW HOLES +POWER BOARD		F：TFT+CONTROL BOARD G：TFT+ SCREW HOLES H：TFT+D/V BOARD I：TFT+ SCREW HOLES +D/V BOARD J：TFT+POWER BD

⑧ Resolution:

A	128160	B	320234	C	320240	D	480234	E	480272	F	640480
G	800480	H	1024600	I	320480	J	240320	K	800600	L	240400
M	1024768	N	128128	P	1280800	Q	480800	R	640320	S	480128
T	800320	U	8001280	V	176220	W	1280398	X	1024250	Y	1920720
Z	800200	2	1024324	3	7201280	4	19201200	5	1366768	6	1280320

⑨ D: Digital L：LVDS M:MIPI

⑩ Interface:

N	Without control board	A	8Bit	B	16Bit	H	HDMI
I	I2C Interface	R	RS232	S	SPI Interface	U	USB

⑪ TS:

N	Without TS	T	Resistive touch panel	C	Capacitive touch panel (G-F-F)
G	Capacitive touch panel (G-G)	C1	Capacitive touch panel (G-F-F)+OCA		
C2	Capacitive touch panel (G-F-F)+OCR	G1	Capacitive touch panel (G-G)+OCA		
G2	Capacitive touch panel (G-G)+OCR	B	CTP+GG+USB		

⑫	Version: X:Raspberry pi	
⑬	Special Code	#:Fit in with ROHS directive regulations

2.Summary

TFT 3.5”is a IPS transmissive type color active matrix TFT liquid crystal display that use amorphous silicon TFT as switching devices. This module is a composed of a TFT_LCD module, It is usually designed for industrial application and this module follows RoHs.

3.General Specifications

Item	Dimension	Unit
Size	3.5	inch
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	76.84(W) x 63.84(H) x 3.27(D)	mm
Active area	70.08 x 52.56	mm
Dot pitch	0.073 x 0.219	mm
LCD type	TFT, normally black, Transmissive	
View Direction	Wide View	
Driver IC	ST7272A or equivalent	
Interface	24-bit RGB	
Aspect Ratio	4:3	
Backlight Type	LED,Normally White	
With /Without TP	Without TP	
Surface	Glare	

*Color tone slight changed by temperature and driving voltage.

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-30	—	+85	℃
Storage Temperature	TST	-40	—	+85	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

5.Electrical Characteristics

5.1. Operating conditions:

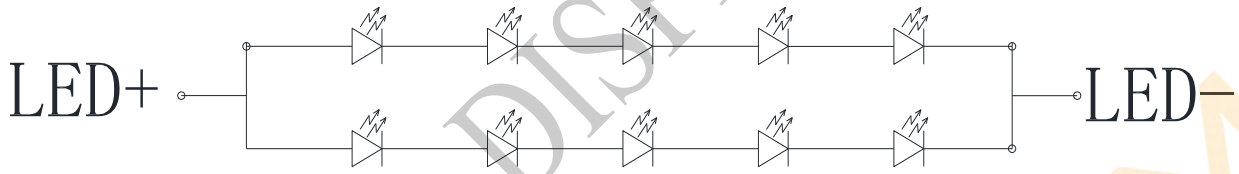
Item	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage For LCM	VCC	3.0	3.3	3.6	V	
Supply Current For LCM	ICC	—	20	30	mA	Note 1

Note 1 : This value is test for VCC =3.3V , Ta=25 ℃ only

5.2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		-	40	-	mA	
Power Consumption		540	600	660	mW	
LED voltage	LED+	13.5	15	16.5	V	Note 1
LED Life Time		-	50,000	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



CIRCUIT DIAGRAM

Note 2 : Ta = 25 ℃
Note 3 : Brightness to be decreased to 50% of the initial value
Note 4 : The single LED lamp case

6.AC Characteristics

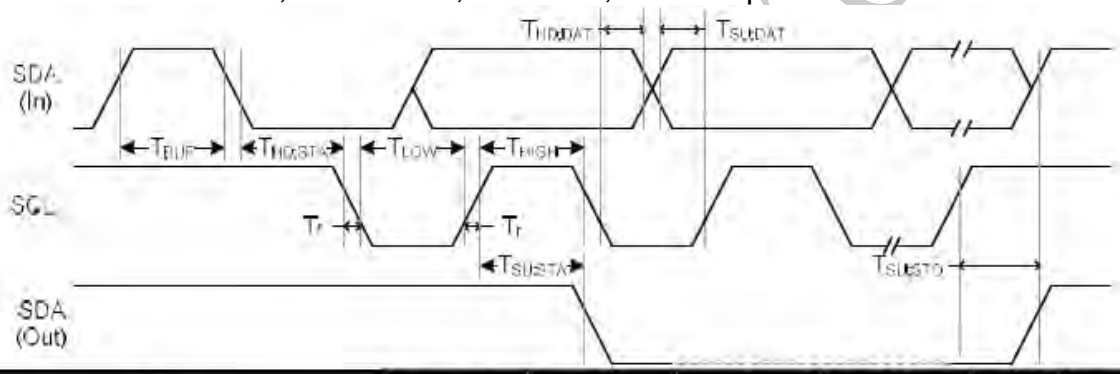
6.1. System Operation AC Characteristics

PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25^{0}C, Bare Chip

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

6.2. System Bus Timing for I2C Interface

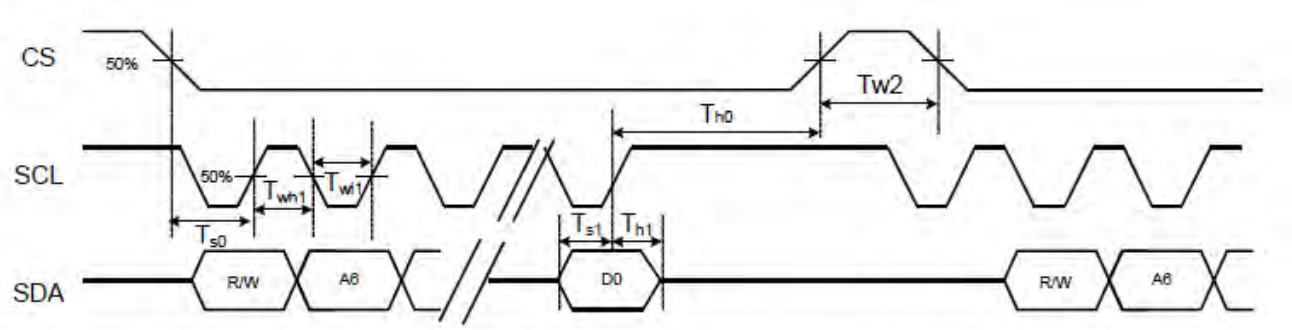
PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25^{0}C, Bare Chip



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL Clock Frequency	FSCL	-	-	400	KHz	
SCL Clock Low Period	TLOW	1300	-	-	ns	
SCL Clock High Period	THIGH	600	-	-	ns	
Signal Rise Time	Tr	20+0.1Cb	-	300	ns	
Signal Fall Time	Tf	20+0.1Cb	-	300	ns	
Start Condition Setup Time	TSU;STA	600	-	-	ns	
Start Condition Hold Time	THD;STA	600	-	-	ns	
Data Setup Time	TSU;DAT	100	-	-	ns	
Data Hold Time	THD;DAT	0	-	900	ns	
Setup Time for STOP Condition	TSU;STO	600	-	-	ns	
Bus Free Time Between a STOP and START	TBUF	100	-	-	ns	
Capacitive load represented by each bus line		Cb		400	pF	

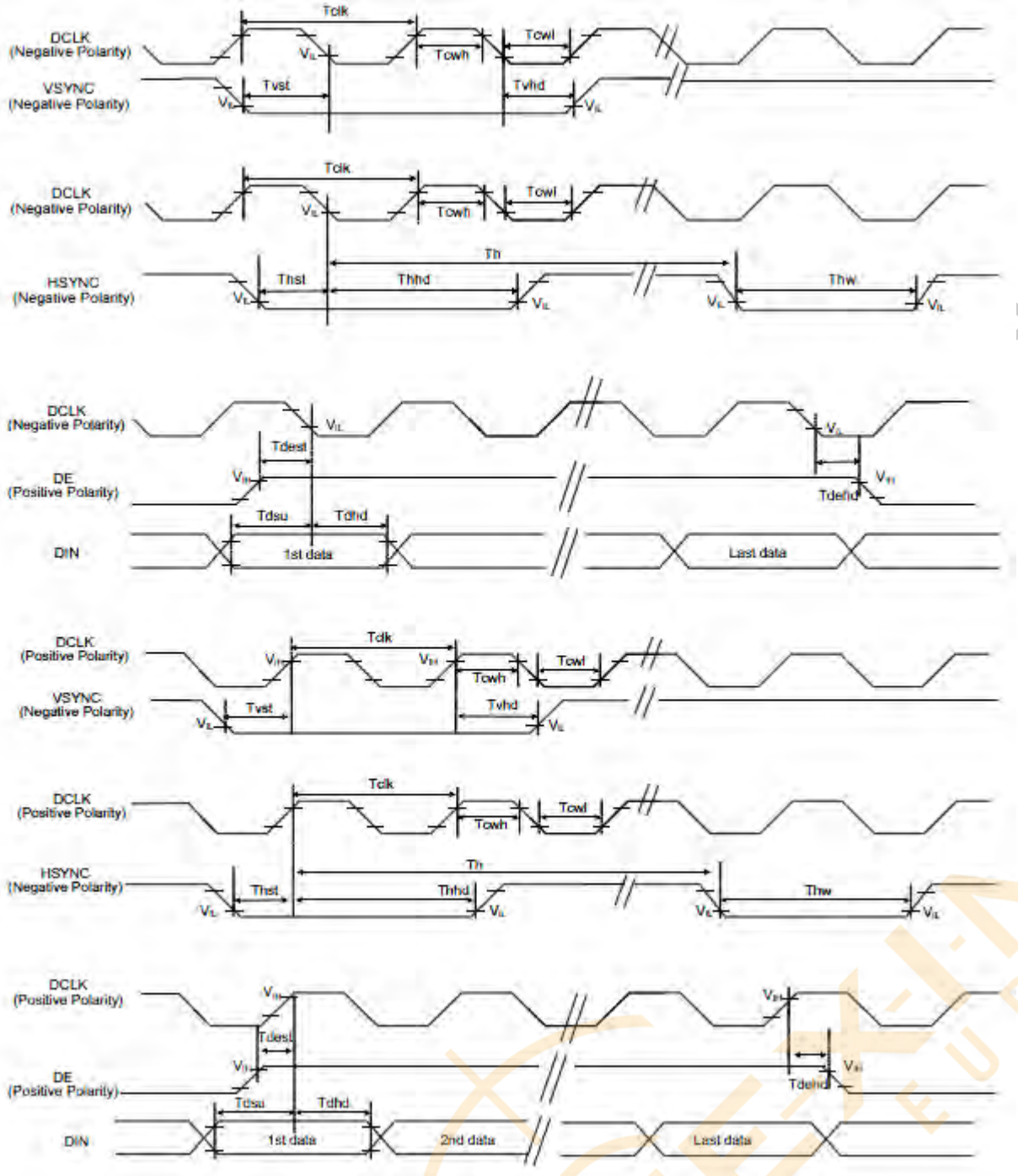
6.3. System Bus Timing for 3-Wire SPI Interface

PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25^{0}C, Bare Chip



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CS Input Setup Time	Ts0	50	-	-	ns	
Serial Data Input Setup Time	Ts1	50	-	-	ns	
CS Input Hold Time	Th0	50	-	-	ns	
Serial Data Input Hold Time	Th1	50	-	-	ns	
SCL Write Pulse High Width	Twh1	50	-	2000	ns	
SCL Write Pulse Low Width	Twl1	50	-	2000	ns	
SCL Read Pulse High Width	Trh1	300		2000	ns	
SCL Read Pulse Low Width	Trl1	300		2000	ns	
CS Pulse High Width	Tw2	400	-	-	ns	

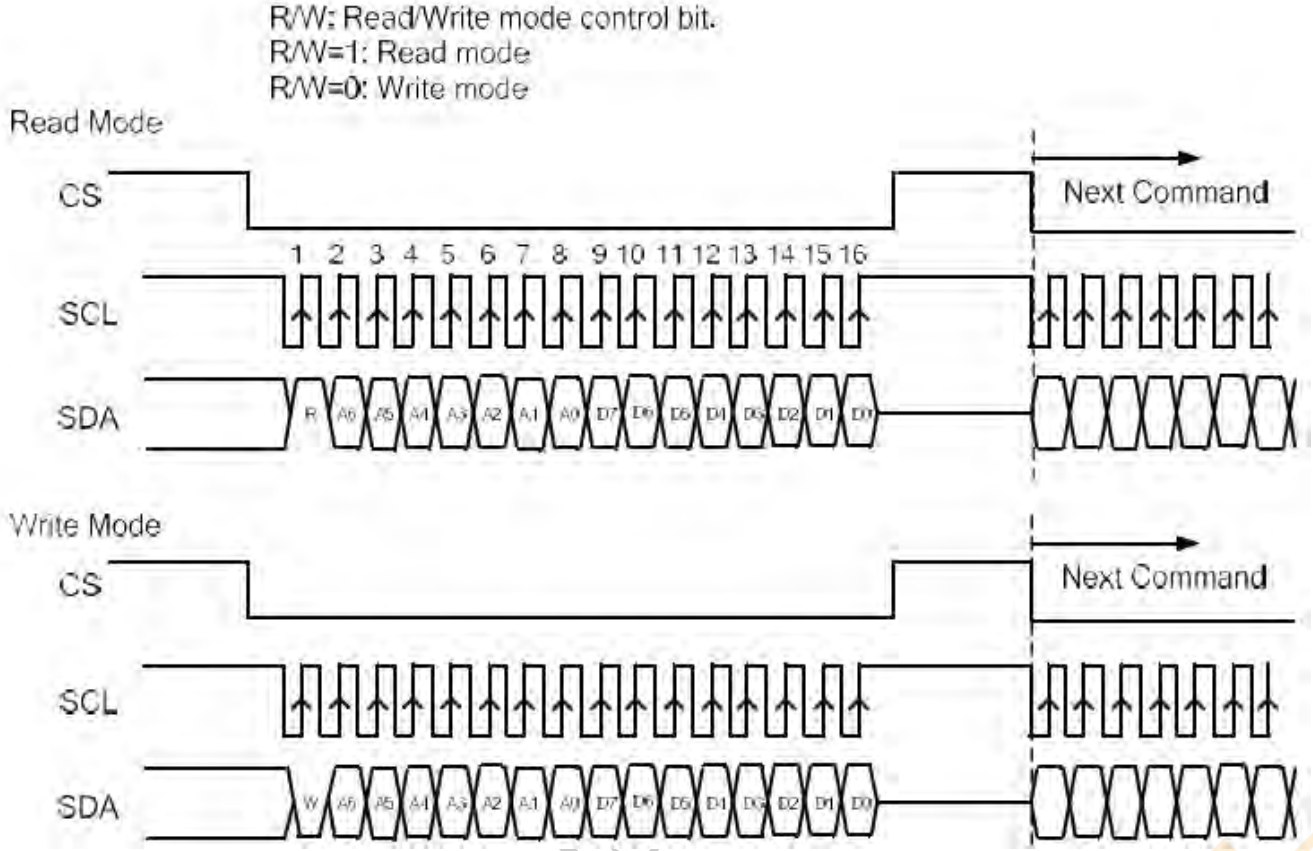
6.4. System Bus Timing for RGB Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tclk	40	50	60	%	
HSYNC Width	Thw	2	-	-	DCLK	
VSYNC Setup Time	Tvst	12	-	-	ns	
VSYNC Hold Time	Tvhd	12	-	-	ns	
HSYNC Setup Time	Thst	12	-	-	ns	
HSYNC Hold Time	Thhd	12	-	-	ns	
Data Setup Time	Tdsu	12	-	-	ns	
Data Hold Time	Tdhd	12	-	-	ns	
DE Setup Time	Tdest	12	-	-	ns	
DE Hold Time	Tdehd	12	-	-	ns	

7.Communication Interface

7.1. 3-wire Serial Interface



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before then rising edge of CS pulse are valid data.

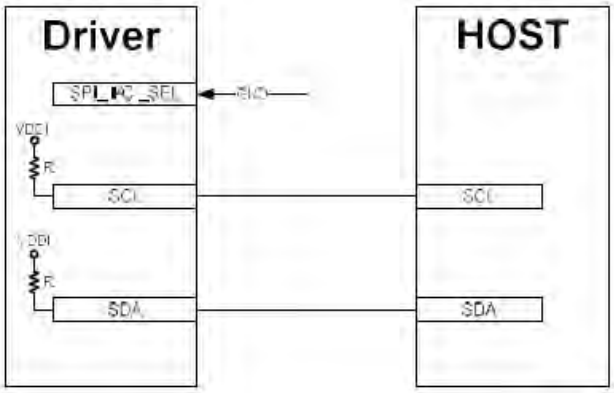
f. Serial block operates with the SCL clock

g. Serial data can be accepted in the power save mode.

h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.

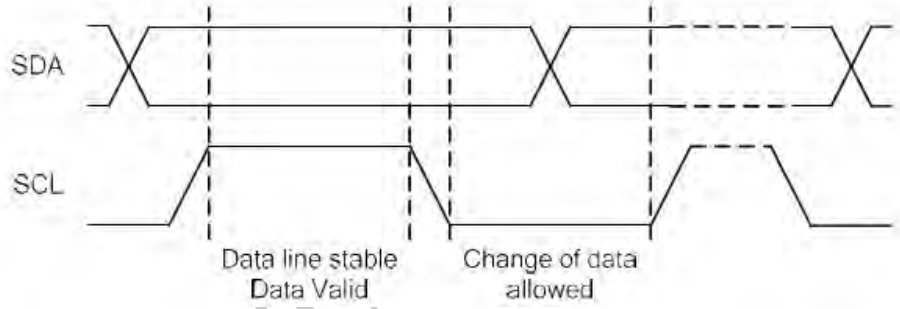
7.2. I2C Interface

The I2C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.



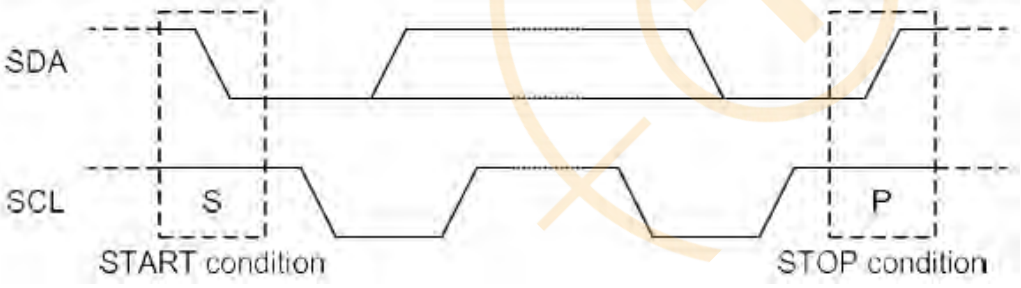
1. Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.

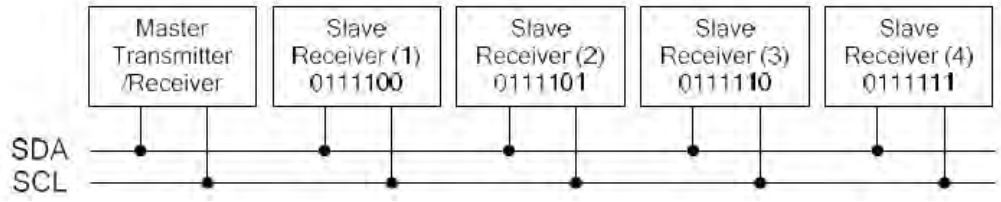


2. START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.



3. System Configuration



The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

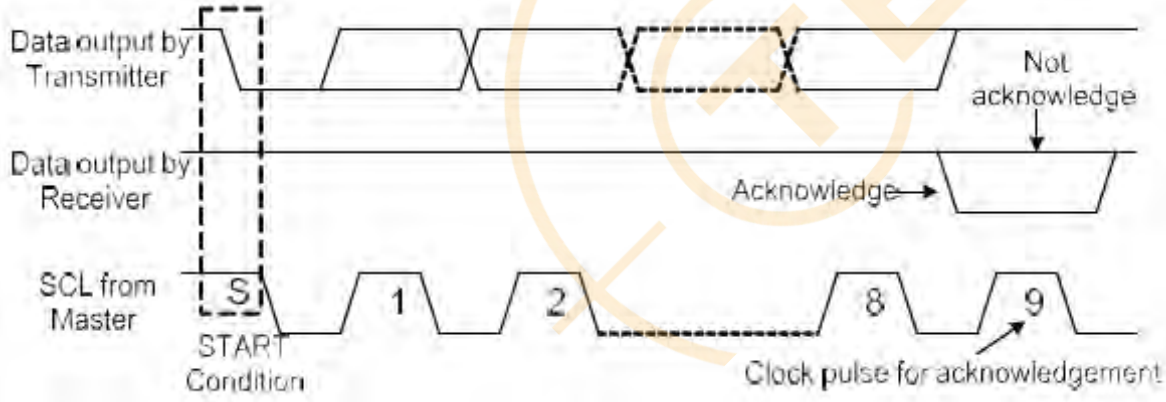
e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.

4.Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledgerelated clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated as follows.

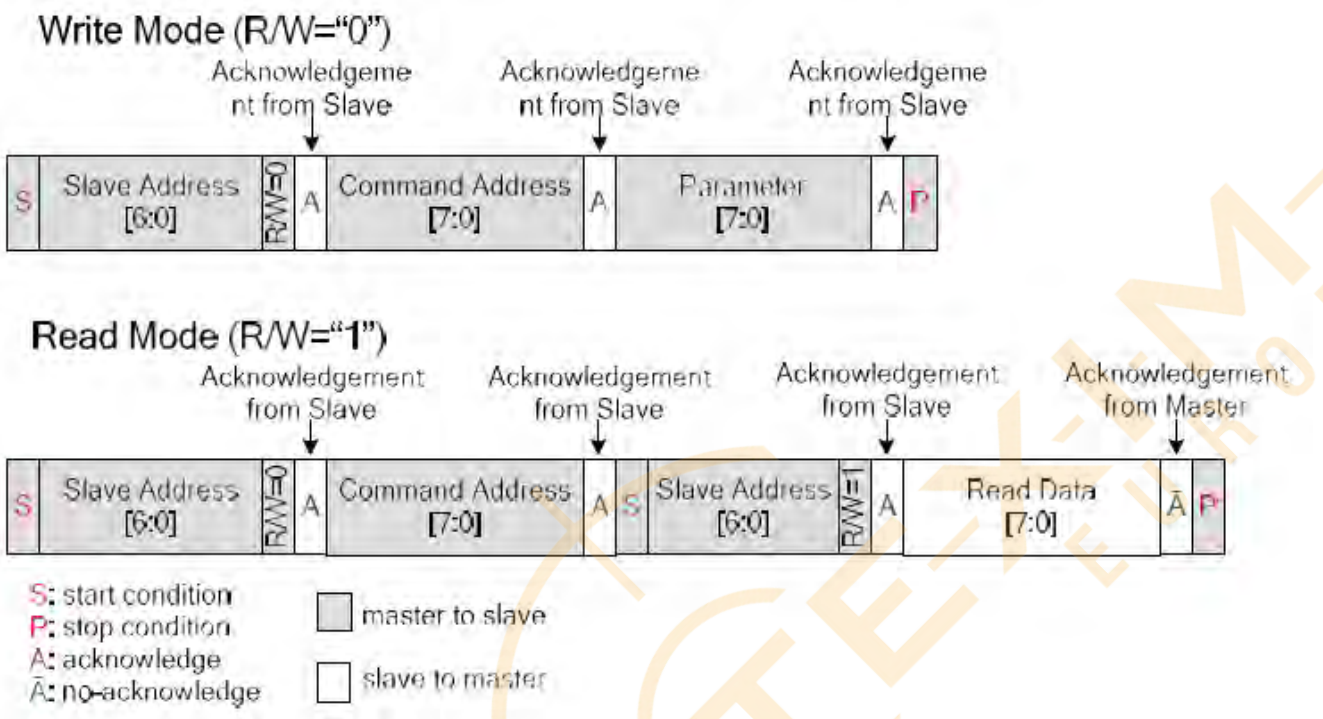


5. I2C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I2C Interface, the device which should respond is addressed first. The default slave address is 0111100b and the three times I2C address could be OTP programing.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.



7.3. RGB Interface

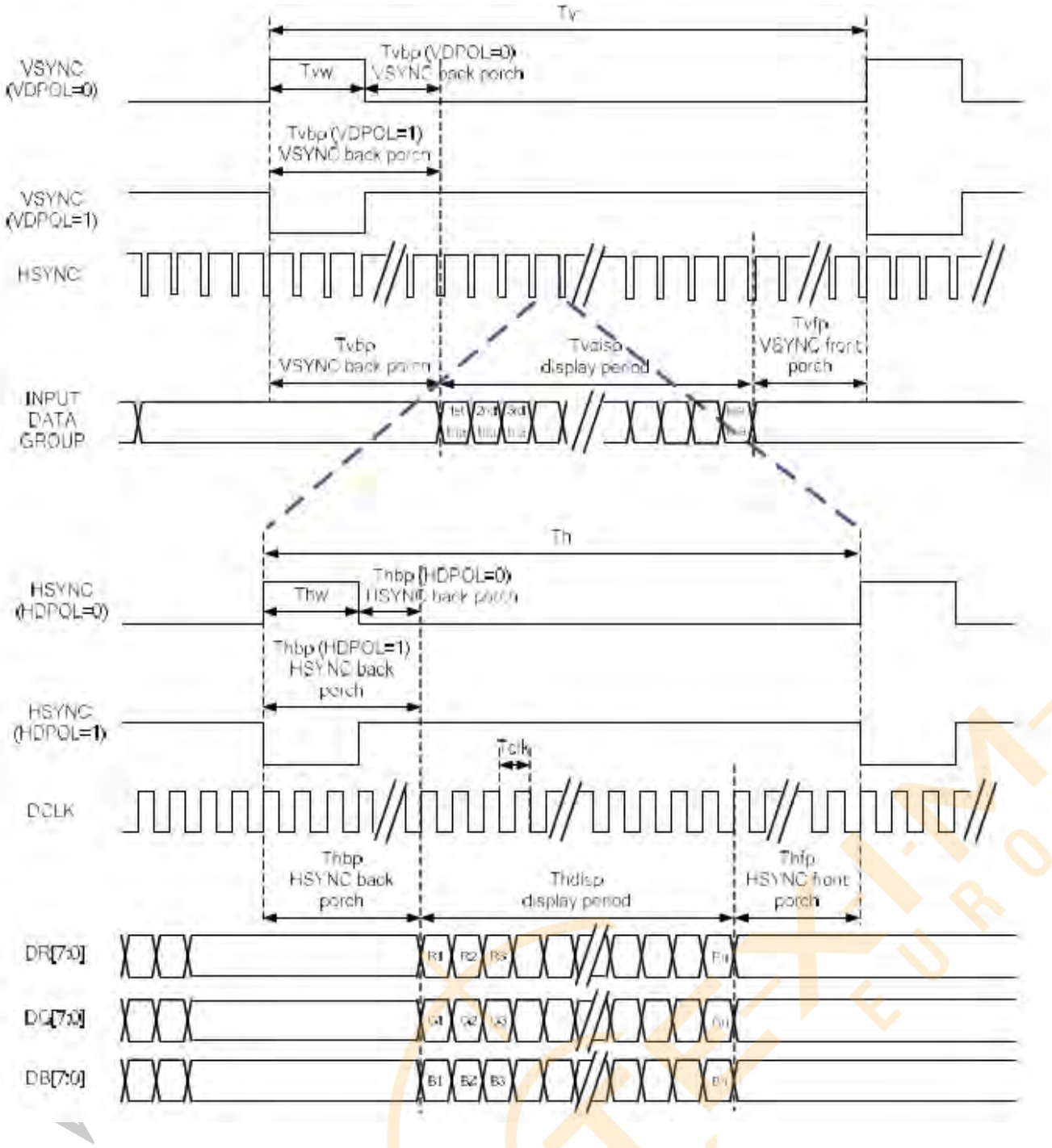
1.Pin Assignment for RGB Interface

Pin		Parallel RGB			Serial RGB		
		888	666	565	888	666	565
VSYNC	SYNC Mode	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	DE Mode	x	x	x	x	x	x
HSYNC	SYNC Mode	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	DE Mode	x	x	x	x	x	x
DE	SYNC Mode	x	x	x	x	x	x
	DE Mode	DE	DE	DE	DE	DE	DE
CLK		CLK	CLK	CLK	CLK	CLK	CLK
DR0		R0	x	x	x	x	x
DR1		R1	x	x	x	x	x
DR2		R2	R0	x	x	x	x
DR3		R3	R1	R0	x	x	x
DR4		R4	R2	R1	x	x	x
DR5		R5	R3	R2	x	x	x
DR6		R6	R4	R3	x	x	x
DR7		R7	R5	R4	x	x	x
DG0		G0	x	x	D0	x	x
DG1		G1	x	x	D1	x	x
DG2		G2	G0	G0	D2	D0	D0
DG3		G3	G1	G1	D3	D1	D1
DG4		G4	G2	G2	D4	D2	D2
DG5		G5	G3	G3	D5	D3	D3
DG6		G6	G4	G4	D6	D4	D4
DG7		G7	G5	G5	D7	D5	D5
DB0		B0	x	x	x	x	x
DB1		B1	x	x	x	x	x
DB2		B2	B0	x	x	x	x
DB3		B3	B1	B0	x	x	x
DB4		B4	B2	B1	x	x	x
DB5		B5	B3	B2	x	x	x
DB6		B6	B4	B3	x	x	x
DB7		B7	B5	B4	x	x	x

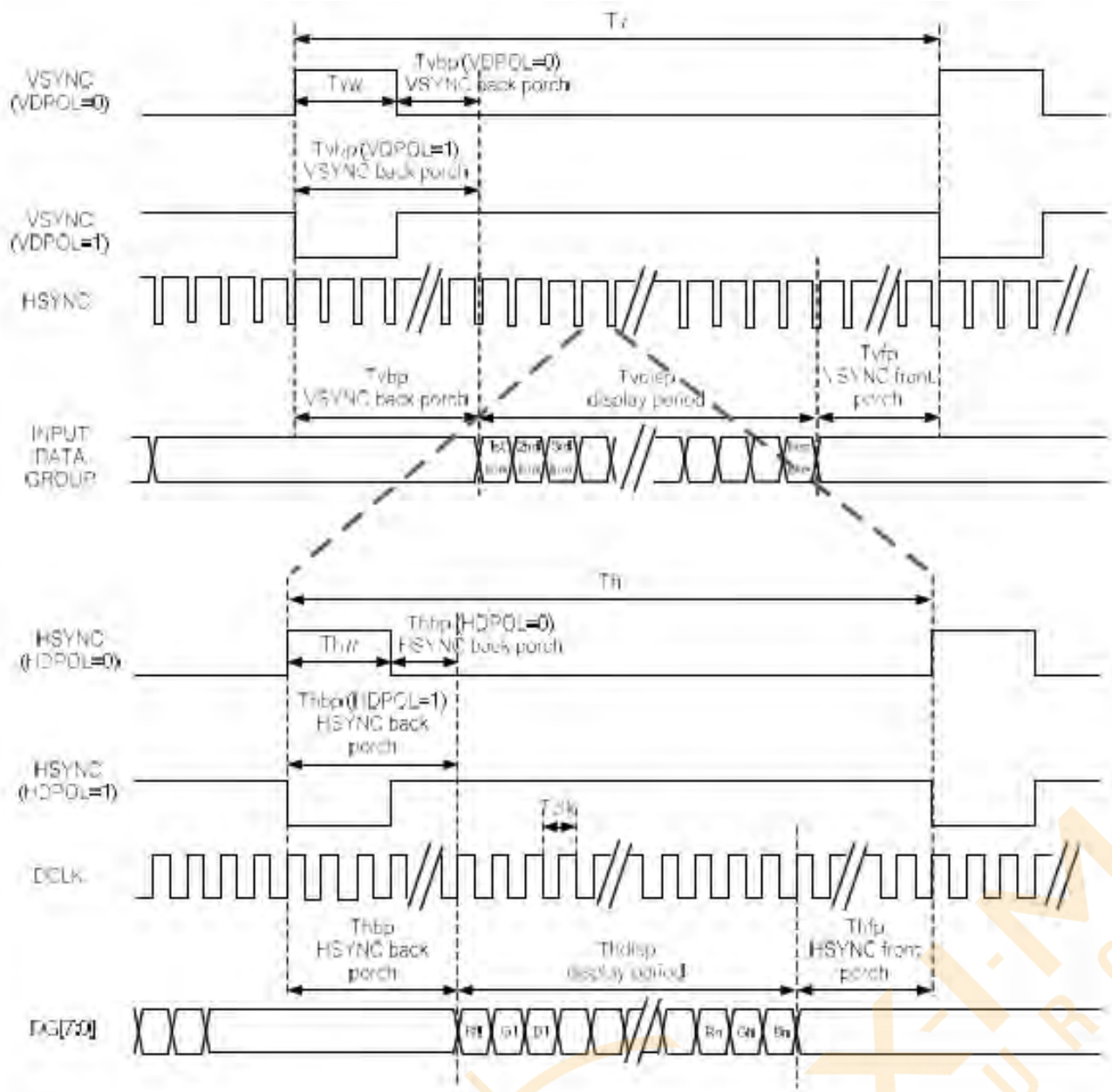
RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC - DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: “Input” means these signals are driven by host side

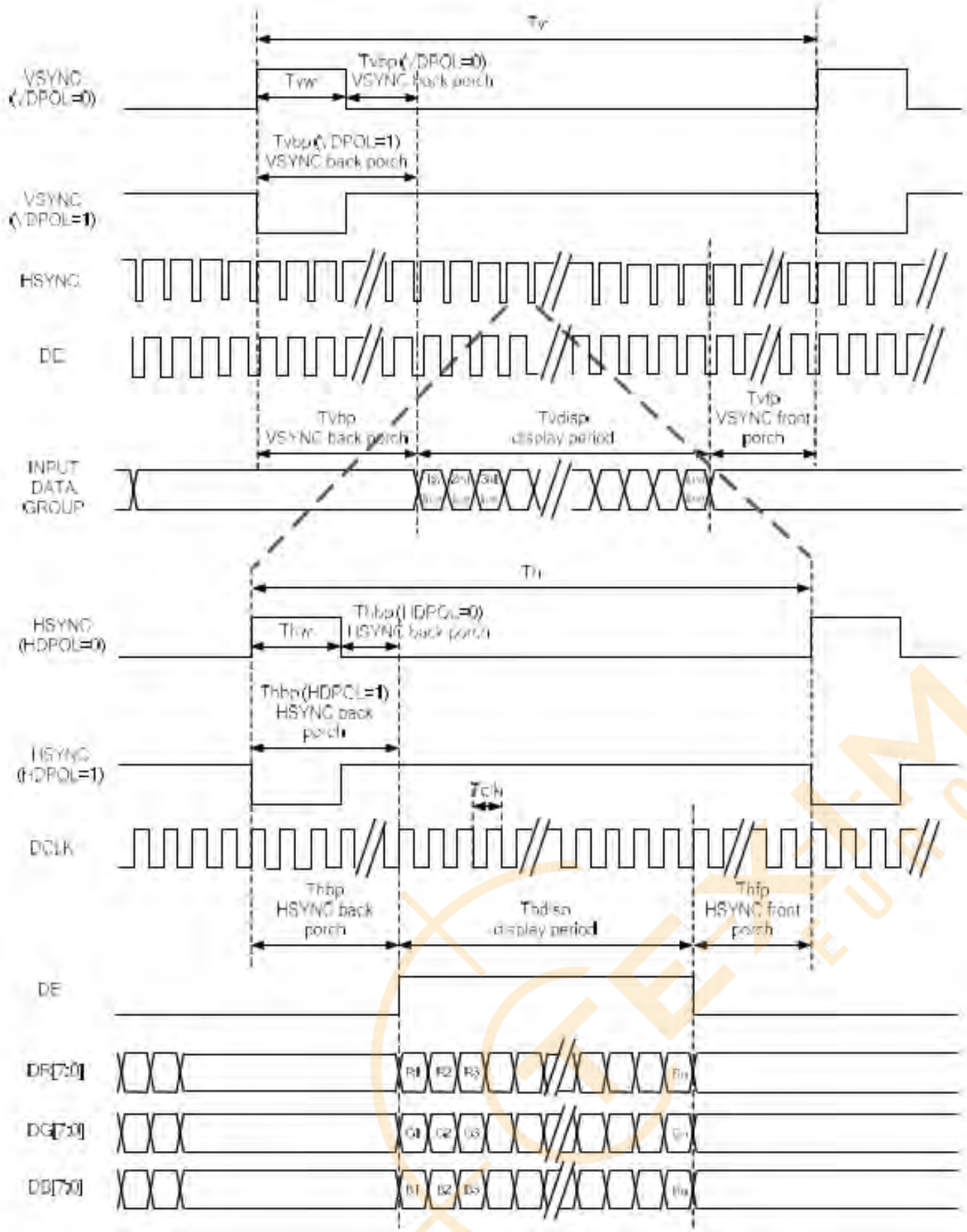
2. Parallel RGB SYNC Mode



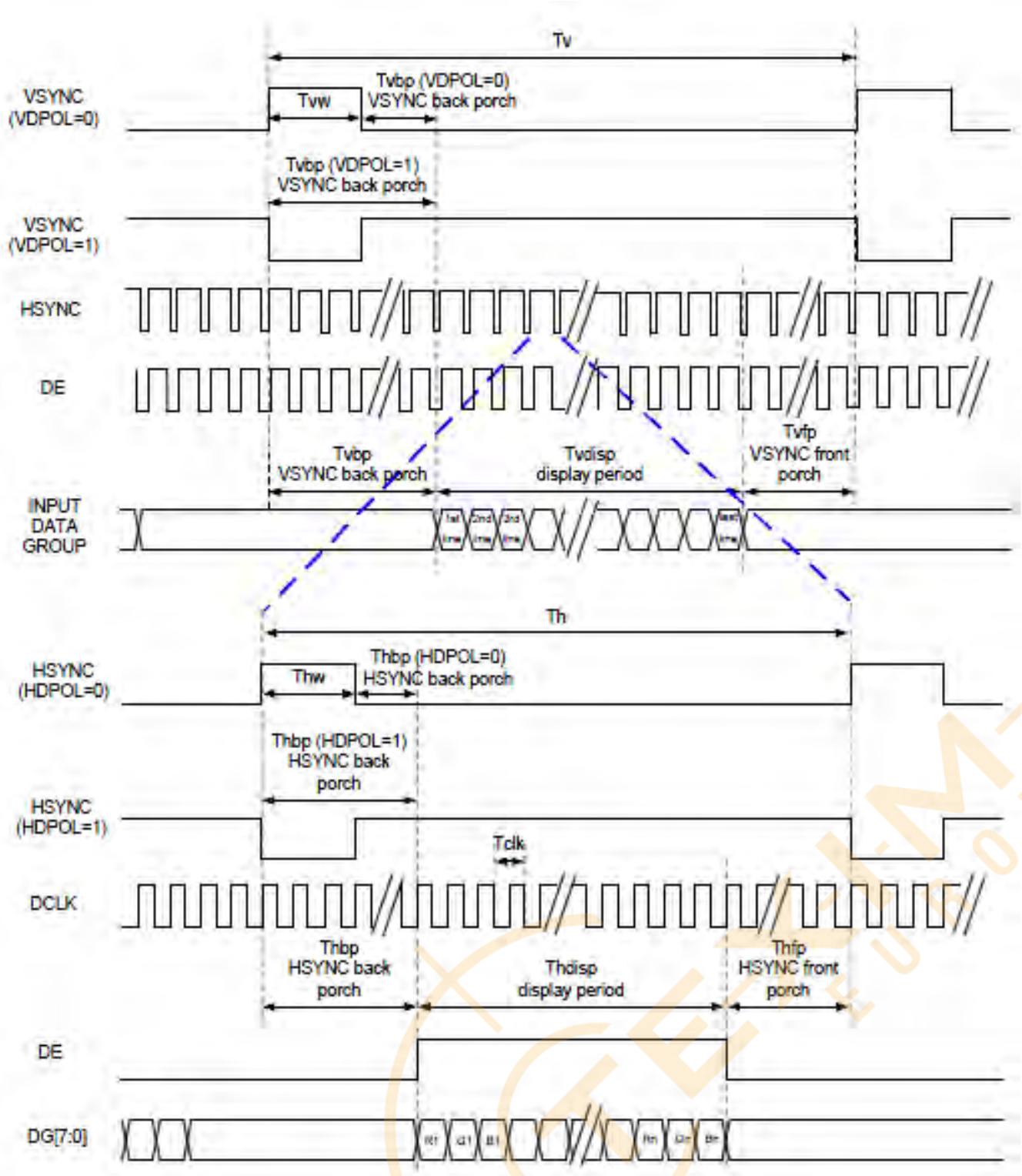
3. Serial RGB SYNC Mode



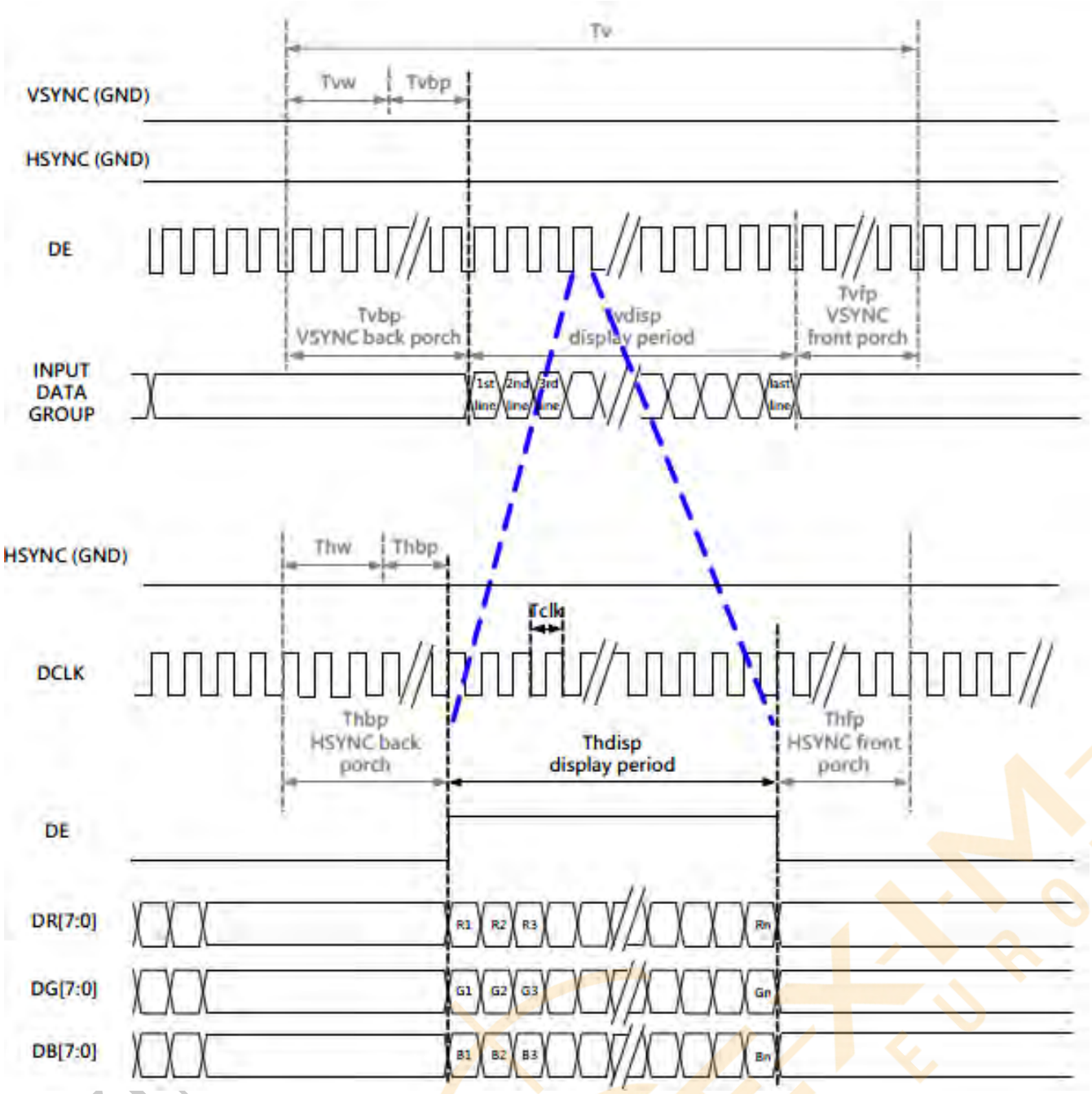
4. Parallel RGB SYNC-DE Mode



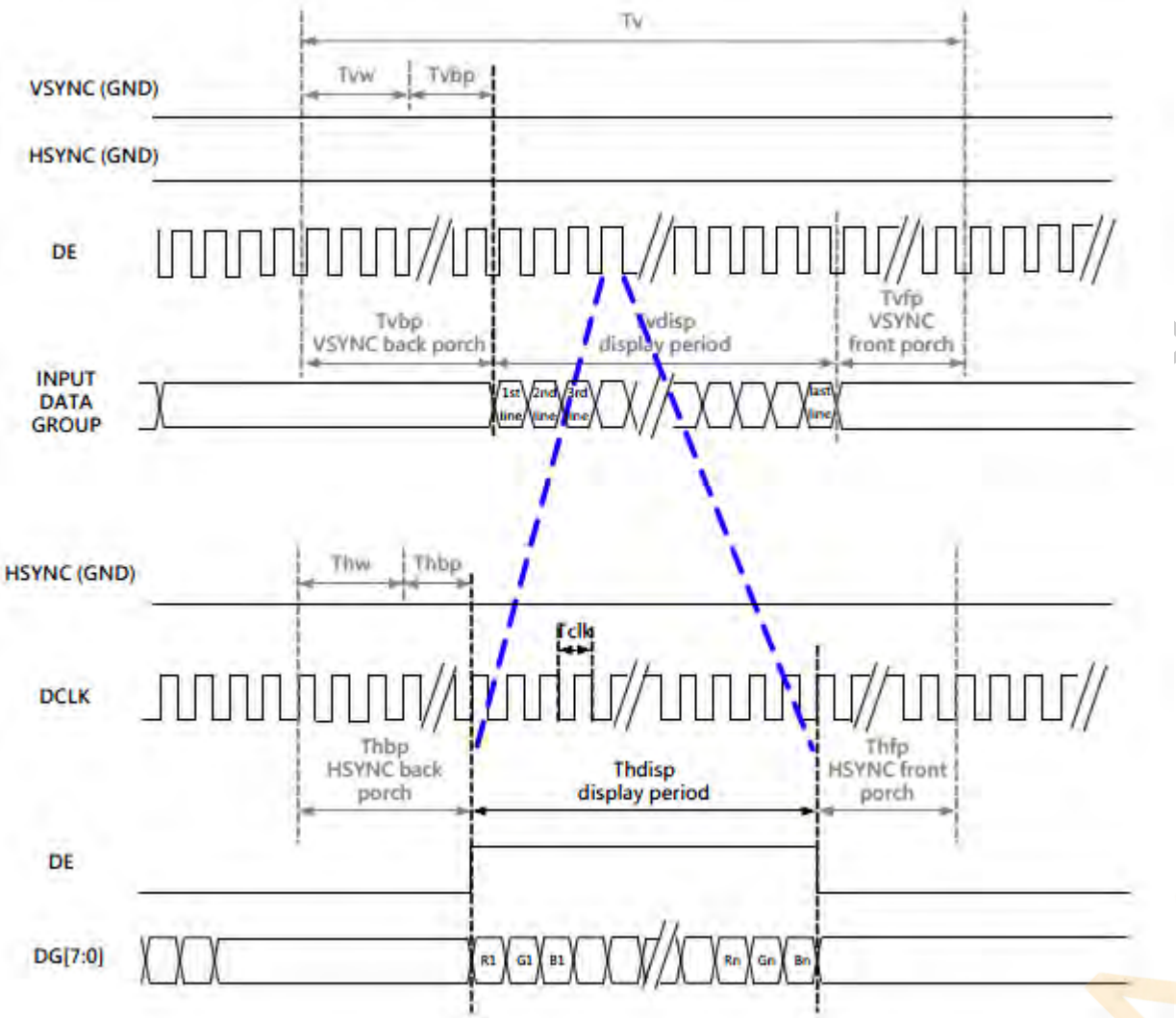
5. Serial RGB SYNC-DE Mode



6. Parallel RGB DE Mode



7. Serial RGB DE Mode



8. Parallel RGB Input Timing Table

Parallel 24-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25 C)

Parallel 24-bit RGB Input Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK Frequency		Fclk	5	6	8	MHz	
DCLK Period		Tclk	125	167	200	ns	
HSYNC	Period Time	Th	325	371	438	DCLK	
	Display Period	Thdisp		320		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	SYNC mode back porch control by H_BLANKING[7:0] setting Thbp= H_BLANKING[7:0]
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	HSYNC	
	Display Period	Tvdisp		240		HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING[7:0] setting Tvbp= V_BLANKING[7:0]
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

9. Serial RGB Input Timing Table

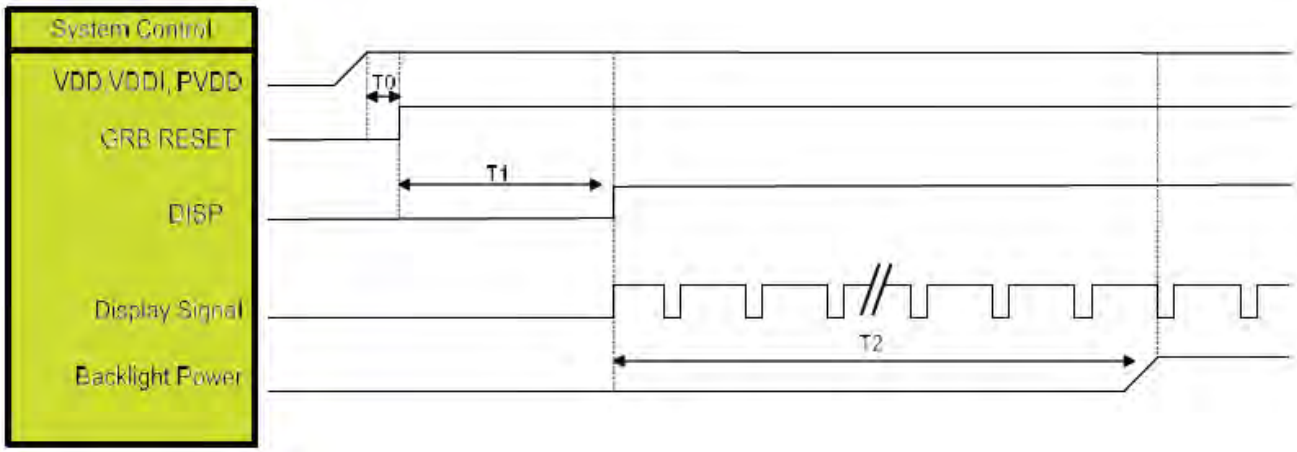
Serial 8-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25 C)

Serial 8-bit RGB Input Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	15	18	21	MHz	
DCLK Period		Tclk	47	55	66	ns	
HSYNC	Period Time	Th	965	1011	1078	DCLK	
	Display Period	Thdisp		960		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	SYNC mode back porch control by H_BLANKING[7:0] setting Thbp= H_BLANKING[7:0]
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	HSYNC	
	Display Period	Tvdisp		240		HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING[7:0] setting Tvbp= V_BLANKING[7:0]
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

7.4. POWER ON/OFF SEQUENCE

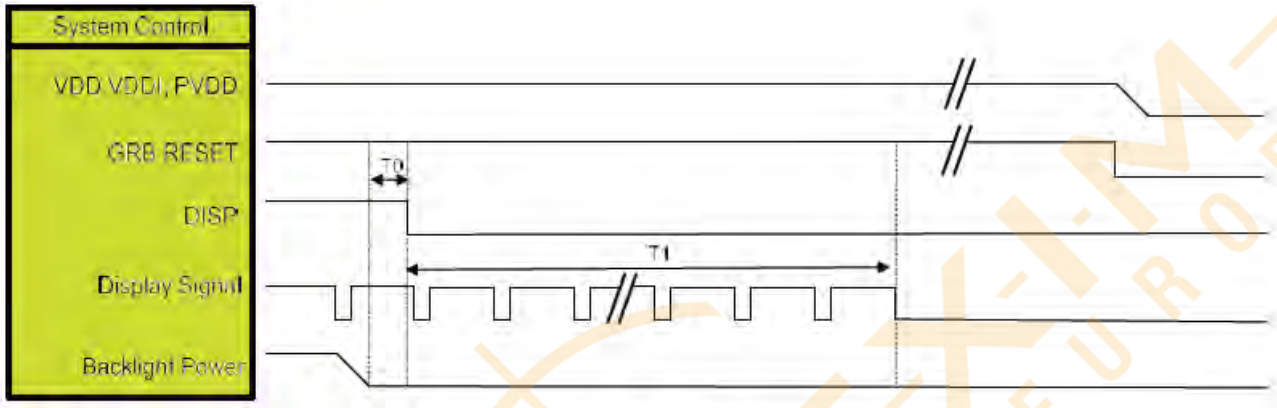
1. Power On Sequence



Symbol	Description	Min. Time	Unit
T0	System power stability to GRB RESET signal	0	ms
T1	GRB RESET= “High” to DISP=”High”	10	ms
T2	Display Signal output to Backlight Power on	250	ms

Note: Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0]

2. Power Off Sequence



Symbol	Description	Min. Time	Unit
T0	Backlight Power off to DISP=”Low”	5	ms
T1	DISP=”Low” to IC internal voltage discharge complete	80	ms

Note: Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0]

8.Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr+ Tf	θ=0°、Φ=0°	-	30	40	ms	Note 3
Contrast ratio		CR	At optimized viewing angle	640	800	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.26	0.31	0.36	-	Note 2,6,7
		Wy		0.30	0.35	0.40	-	
Viewing angle	Hor.	ΘR	CR≧10	70	80	-	Deg.	Note 1
		ΘL		70	80	-		
	Ver.	ΦT		70	80	-		
		ΦB		70	80	-		
Brightness		-	-	1000	-	-	cd/m^2	Center of display
Uniformity		(U)	-	75	-	-	%	Note 5

Ta=25±2℃, IL=40mA

Note 1: Definition of viewing angle range

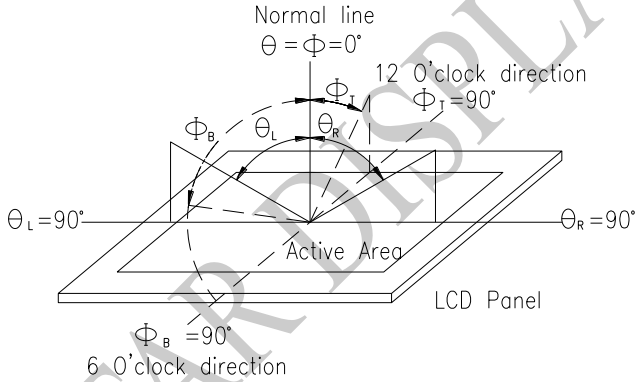


Fig. 8.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

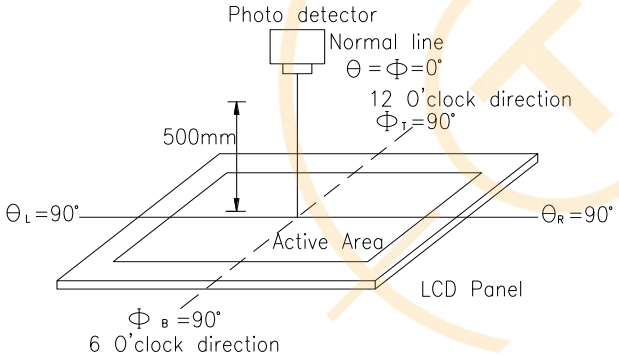
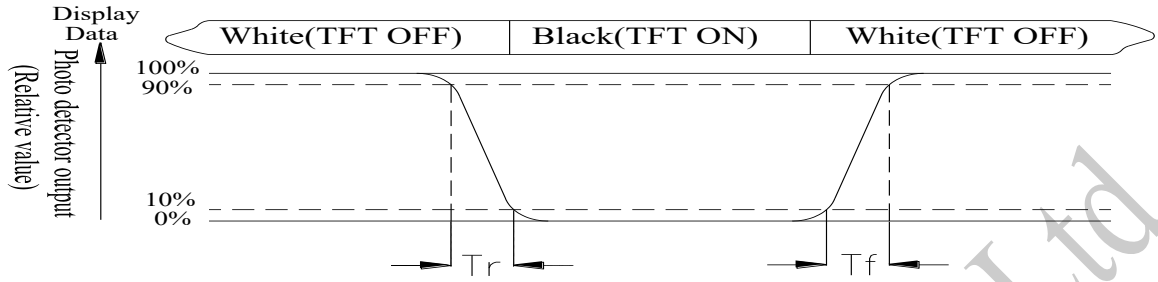


Fig. 8.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

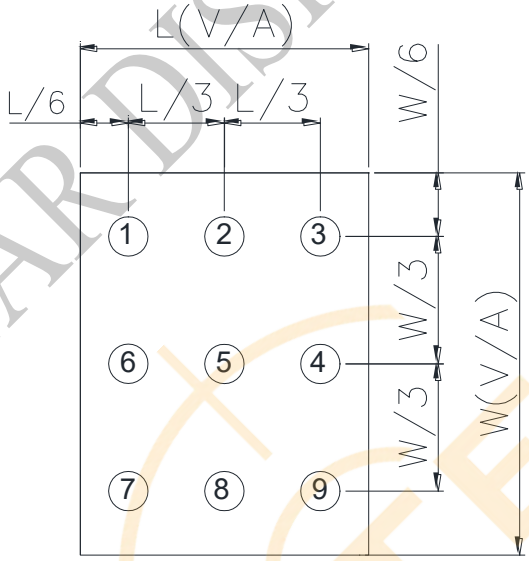


Fig8.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

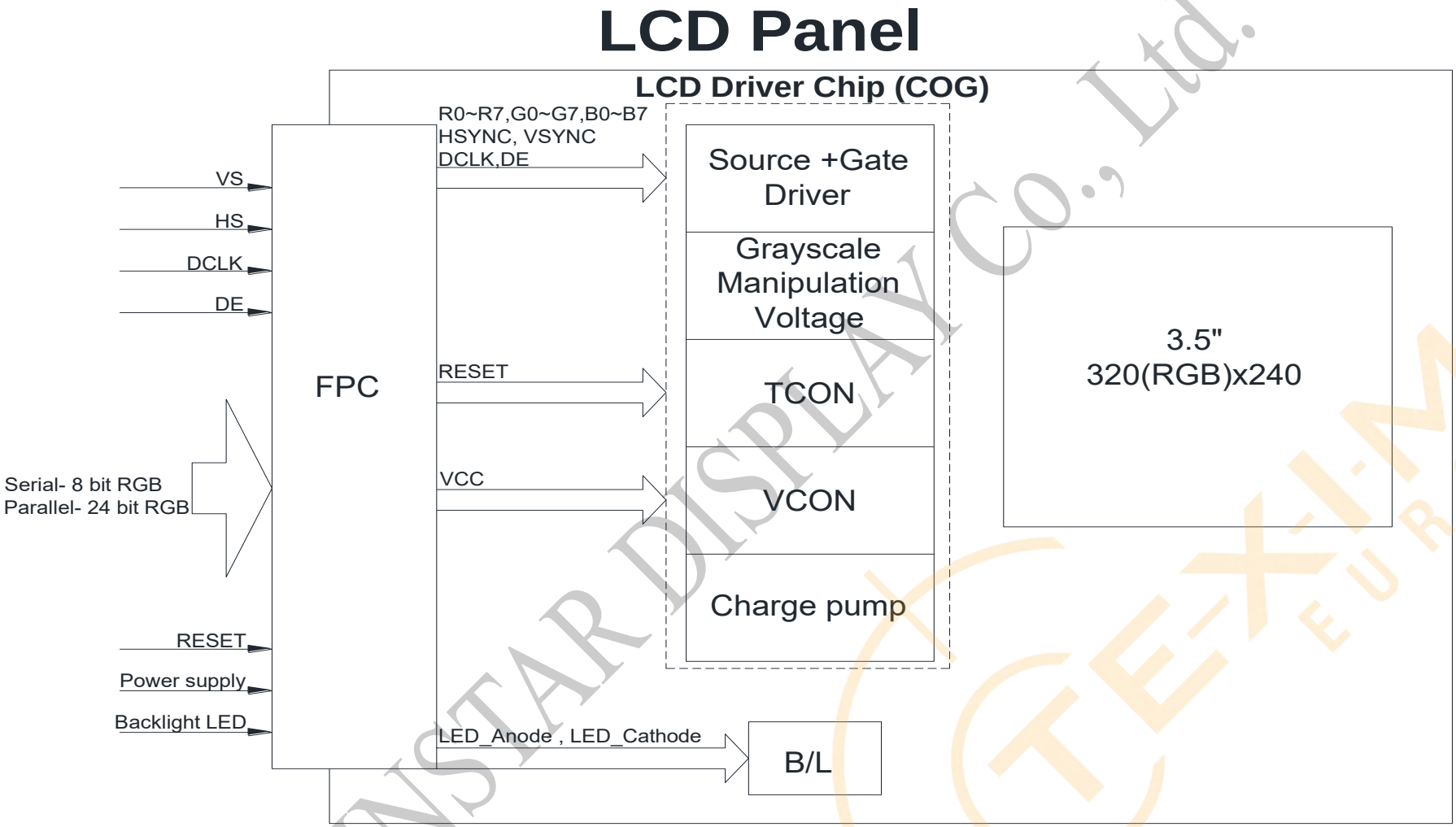
9.Interface

9.1. LCM PIN Definition

Pin	Symbol	Function	Remark
1	LED-	Power for LED backlight cathode	
2	LED-	Power for LED backlight cathode	
3	LED+	Power for LED backlight anode	
4	LED+	Power for LED backlight anode	
5	NC(YU)	No connect	
6	NC(XL)	No connect	
7	NC(SPI_IIC_SEL)	No connect	
8	/RESET	Hardware reset	
9	NC(CS)	No connect	
10	NC(SDA)	No connect	
11	NC(SCL)	No connect	
12	B0	Data bus	
13	B1	Data bus	
14	B2	Data bus	
15	B3	Data bus	
16	B4	Data bus	
17	B5	Data bus	
18	B6	Data bus	
19	B7	Data bus	
20	G0	Data bus	
21	G1	Data bus	
22	G2	Data bus	
23	G3	Data bus	
24	G4	Data bus	
25	G5	Data bus	
26	G6	Data bus	
27	G7	Data bus	
28	R0	Data bus	
29	R1	Data bus	
30	R2	Data bus	

31	R3	Data bus	
32	R4	Data bus	
33	R5	Data bus	
34	R6	Data bus	
35	R7	Data bus	
36	HSYNC	Horizontal sync signal, default is negative polarity.	
37	VSYNC	Vertical sync signal, default is negative polarity.	
38	DCLK	Dot-clock signal and oscillator source	
39	NC(HDIR)	No connect	
40	NC(VDIR)	No connect	
41	VCC	Power Supply	
42	VCC	Power Supply	
43	NC(YD)	No connect	
44	NC(XR)	No connect	
45	NC(PARA_SERI)	No connect	
46	NC(BIST_EN)	No connect	
47	NC(ENPROG)	No connect	
48	NC	No connect	
49	NC	No connect	
50	NC	No connect	
51	NC(DISP)	No connect	
52	DE	Data input enable. Display access is enabled when DE is “H”.	
53	GND	Ground	
54	GND	Ground	

10.Block Diagram



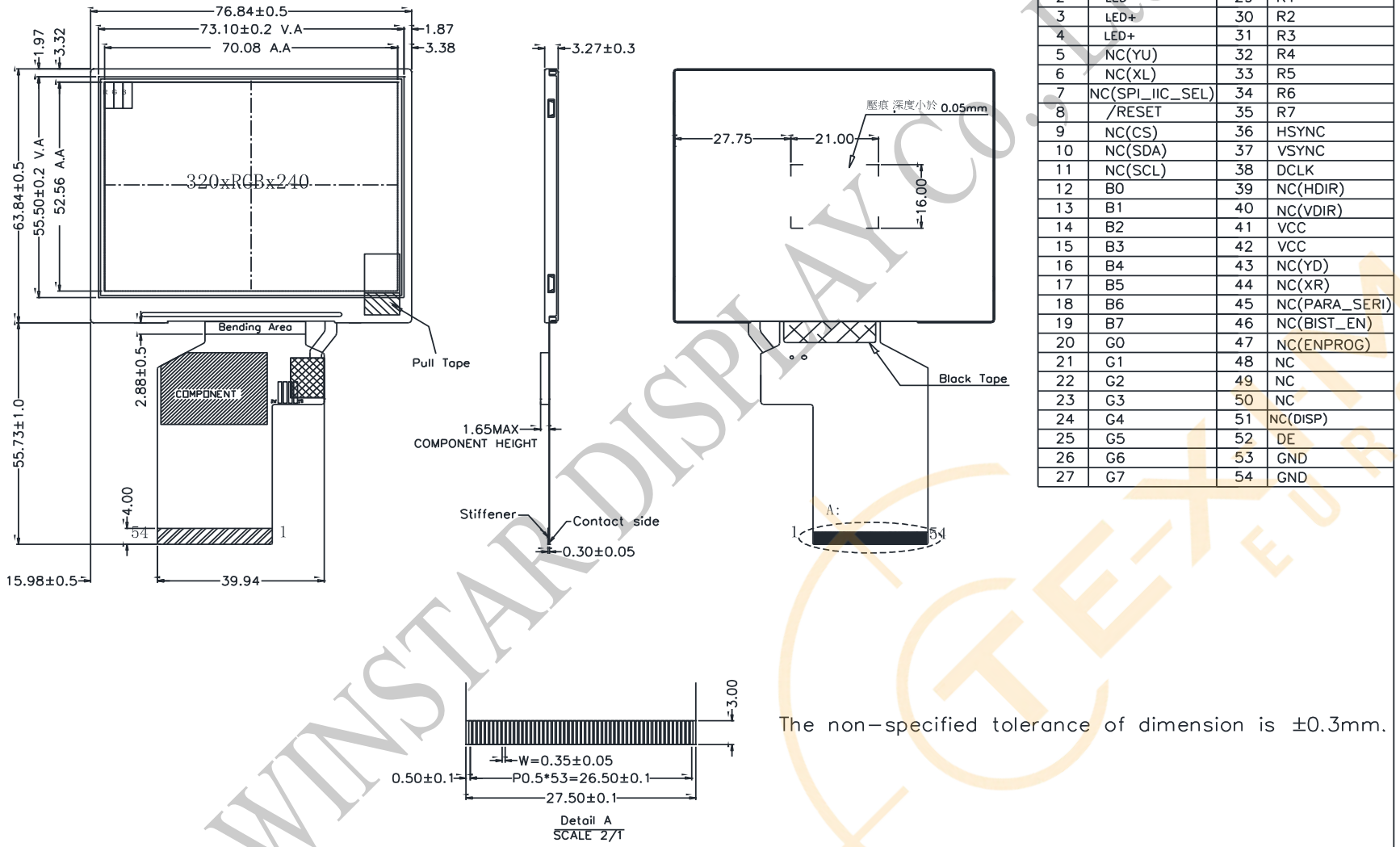
11.Reliability

Content of Reliability Test (Super Wide temperature, -30℃~85℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	85℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-40℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30℃ 200hrs	1
High Temperature/ Humidity storage	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -30℃ 25℃ 85℃ 30min 5min 30min 1 cycle	-30℃/85℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	**3**
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact), ±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.
Note3: The packing have to including into the vibration testing.

12.Contour Drawing



PinNo.	Symbol	PinNo.	Symbol
1	LED-	28	R0
2	LED-	29	R1
3	LED+	30	R2
4	LED+	31	R3
5	NC(YU)	32	R4
6	NC(XL)	33	R5
7	NC(SPI_IIC_SEL)	34	R6
8	/RESET	35	R7
9	NC(CS)	36	HSYNC
10	NC(SDA)	37	VSYNC
11	NC(SCL)	38	DCLK
12	B0	39	NC(HDIR)
13	B1	40	NC(VDIR)
14	B2	41	VCC
15	B3	42	VCC
16	B4	43	NC(YD)
17	B5	44	NC(XR)
18	B6	45	NC(PARA_SERI)
19	B7	46	NC(BIST_EN)
20	G0	47	NC(ENPROG)
21	G1	48	NC
22	G2	49	NC
23	G3	50	NC
24	G4	51	NC(DISP)
25	G5	52	DE
26	G6	53	GND
27	G7	54	GND

The non-specified tolerance of dimension is ±0.3mm.

13.檢驗規範(Inspection Specification)

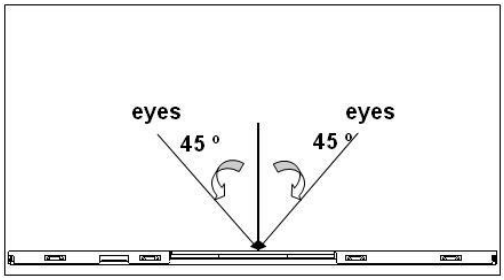
1. 範圍(Scope)：適用於本公司 TFT-LCD 模塊(The document shall be applied to TFT-LCD Module)
2. 檢驗標準(Inspection Standard)：MIL-STD-105E 正常單次抽樣水平 II(MIL-STD-105E Table Normal Inspection Single Sampling Level II)
3. 缺陷水平(Defect Level)：主要缺陷 AQL：0.65;次要缺陷 AQL：2.5(Major Defect AQL:0.65;Minor Defect AQL:2.5)
4. 檢驗條件(Test conditions):

   (1)溫度(Temperature)：15℃~25℃ ；溼度(Humidity)：55 ±15%

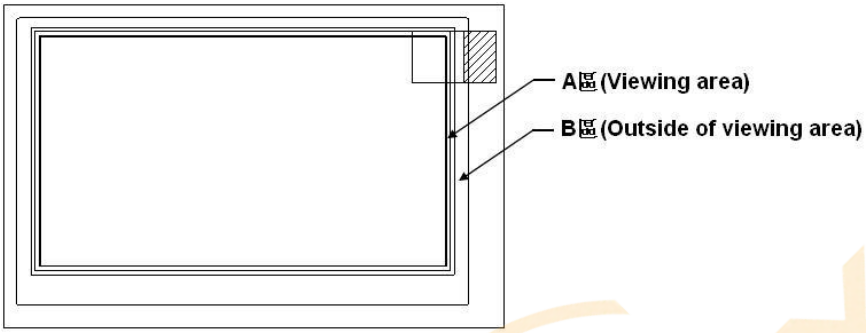
   (2)外觀檢驗(Visual inspection)：光照強度：500 Lux 以上;檢查距離：20cm~30cm (Illumination：More than 500 Lux; Inspection Distance: 20cm~30cm)

   (3)電性檢驗(Electrical inspection)：光照強度：100Lux~300Lux;檢查距離：20cm~30cm(Illumination：100Lux~300Lux; Inspection Distance: 20cm~30cm)

   (4)目視角度(Visual angle)：檢查目視的角度是法線方法的 45 º(The test direction is base on about around 45º of Vertical line）



(5)定義區域(Definition of area):



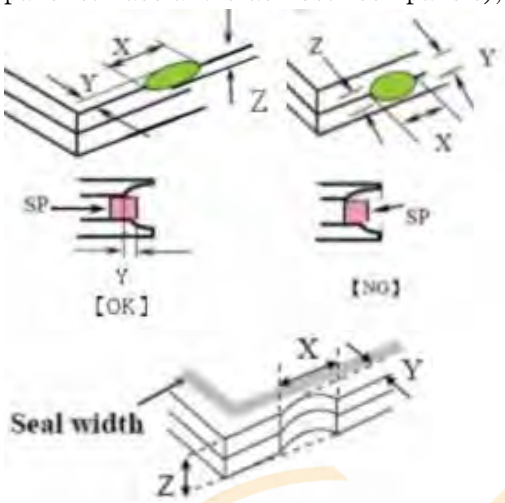
5. 象素定義 (Pixel Definition):

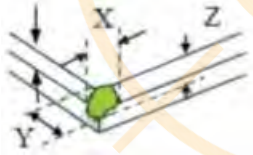
R	G	B	R	G	B	R	G	B		Dot Defect
R	G	B	R	G	B	R	G	B		Adjacent Dot Defect
R	G	B	R	G	B	R	G	B		Cluster

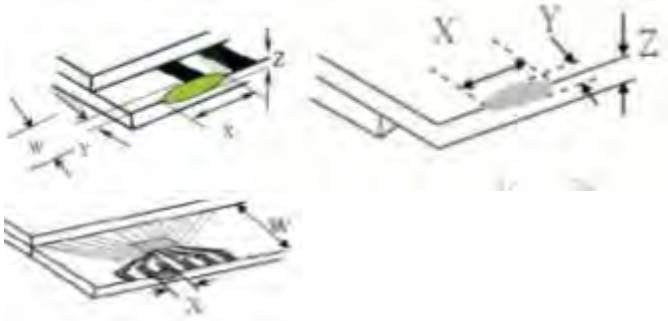
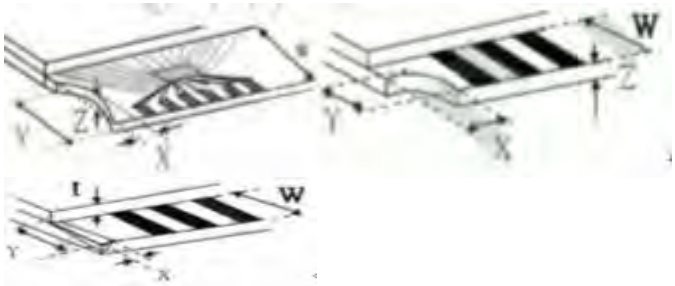
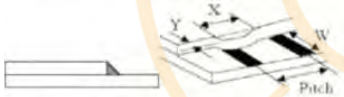
Note 1:If pixel or partial sub-pixel defects exceed 50% of the affected pixel or sub-pixel area, it shall be considered as1 defect.

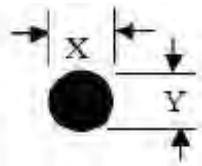
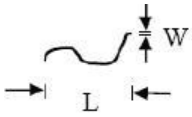
Note 2: There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

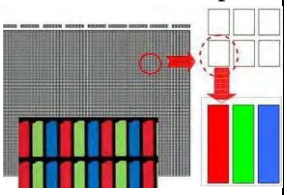
5. 檢驗標準(Inspection Standard)：

<table>
<tr><th>項次
(No)</th><th>檢驗項目(Inspection item)</th><th>檢驗標準(Inspection Standard)</th><th>缺陷等級
(Defect Level)</th></tr>
<tr><td>1</td><td>PACKING
&INDICATE</td><td>1.1.不可有混入其他型號產品的現象(Mixde product types).
1.2.不可有產品漏工序的現象(The part number is inconsistent with work order of production).
1.3.不可有部件裝反方向的現象(Assembled in inverse direction).
1.4.不可有數量與實際要求不一致的現象(The quantity is inconsistent with work order of production).</td><td>主缺
(Maj)</td></tr>
<tr><td>2</td><td>尺寸(Size)</td><td>产品尺寸和结构必须符合结构图(Product size and structure must meet the structure diagram)</td><td>主缺
(Maj)</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">玻璃裂纹(The crack of glass)</td><td>符號(Symbols):
X:破裂長度(Symbols)
Y:破裂寬度(The width of crack).
Z:破裂厚度(The thickness of crack).
W:出電極區寬度(Terminal length)
T:玻璃厚度(The thickness of glass).
a:LCD 側面長度(LCD side length).</td><td rowspan="3">次缺
(Min)</td></tr>
<tr><td>3.1.一般玻璃破損(General glass chip):
3.1.1.玻璃表面或上、下玻璃組合縫隙之間破損(Chip on panel surface and crack between panels);
 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤a</td><td>裂紋進入 VA 區(Crack can't enter viewing area)</td><td>≤1/2t</td></tr>
<tr><td>≤a</td><td>裂紋超過 SP 一半的寬度(Crack can't exceed the half of SP width)</td><td>1/2t＜Z≤2t</td></tr>
</table></td></tr>
<tr><td>3.1.2.邊角破損(Corner crack)：
 
</td></tr>
</table>

<table>
<tr><th>項次
(No)</th><th>檢驗項目(Inspection item)</th><th>檢驗標準(Inspection Standard)</th><th>缺陷等級
(Defect Level)</th></tr>
<tr><td>3</td><td>玻璃裂纹(The crack of glass)</td><td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤1/5a</td><td>裂紋進入 VA 區(Crack can't enter viewing area)</td><td>≤1/2t</td></tr>
<tr><td>≤1/5a</td><td>裂紋超過 SP 一半的寬度(Crack can't exceed the half of SP width)</td><td>1/2t＜Z≤2t</td></tr>
</table>
3.2.出电极端破损(Protrusion over terminal):
3.2.1.电极垫上破损(Chip on electrode pad):

<table>
<tr><th>位置(Position)</th><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>正面(Front)</td><td>≤a</td><td>≤1/2W</td><td>≤t</td></tr>
<tr><td>背面(Back)</td><td>≤a</td><td>≤W</td><td>≤1/2t</td></tr>
</table>
3.2.2.出電極端非電極破損(Non-conductive portion):

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤1/3a</td><td>≤W</td><td>≤t</td></tr>
</table>
備註(Note)：
如果破碎部分触及 ITO 電極則不可超過 ITO 電極寬度的 1/3，且必須進行通電測試，不可影響顯示效果(If the chipped area touches the ITO terminal,over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications).
3.2.3.玻璃破損(Glass remain)：

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤a</td><td>≤1/3W</td><td>≤t</td></tr>
</table>
</td><td>次缺
(Min)</td></tr>
</table>

<table>
<tr><th>項次
(No)</th><th>檢驗項目(Inspection item)</th><th>檢驗標準(Inspection Standard)</th><th>缺陷等級
(Defect Level)</th></tr>
<tr><td>4</td><td>黑點、白點異物
(Black or white dot)Round type
 
</td><td>4.1 Round type(Non-display or display):
<table><tr><th>尺寸
(Size)</th><th>判定標準(Judging standard)</th><th>允收數量
(Acceptance(Q'ty))</th></tr><tr><td rowspan="3">1.44”
~4.9”</td><td>D ≤0.25mm</td><td>忽略不計(Ignore)</td></tr><tr><td>0.25mm < D ≤ 0.5mm</td><td>N≦3</td></tr><tr><td>D > 0.5mm</td><td>N≦0</td></tr></table>distance >=5mm</td><td>次缺
(Min)</td></tr>
<tr><td>5</td><td>刮痕、線狀異物
(scratch、contamination)
Line type
 
</td><td>5.1 Line type(Non-display or display):
<table><tr><th>尺寸
(Size)</th><th colspan="2">判定標準(Judging standard)</th><th>允收數量
(Acceptance(Q'ty))</th></tr><tr><td rowspan="4">1.44”
~7.0”</td><td>W</td><td>L</td><td rowspan="2"></td></tr><tr><td>W≦ 0.05mm</td><td>—</td><td>忽略不計(Ignore)</td></tr><tr><td>0.05mm＜W≦0.1mm</td><td>L ≦ 5mm</td><td>N≦3</td></tr><tr><td>W ＞ 0.1mm</td><td>L ＞ 5mm</td><td>N≦0</td></tr></table>distance >=5mm</td><td>次缺
(Min)</td></tr>
<tr><td>6</td><td>POL 氣泡(Polarizer Bubble)</td><td><table><tr><th>視區(area)</th><th>判定標準(Judging standard)</th><th>允收數量
(Acceptance(Q'ty))</th></tr><tr><td rowspan="4">A 區
(Viewing area)</td><td>D < 0.2 mm</td><td>忽略不計(Ignore)</td></tr><tr><td>0.2mm＜D≦0.3mm</td><td>N≦3</td></tr><tr><td>0.3mm＜D≦0.5mm</td><td>N≦1</td></tr><tr><td>0.5mm＜D</td><td>N≦0</td></tr><tr><td>B 區(Outside of viewing area)</td><td>_</td><td>忽略不計(Ignore)</td></tr></table></td><td>次缺
(Min)</td></tr>
<tr><th>項次
(No)</th><th>檢驗項目(Inspection item)</th><th>檢驗標準(Inspection Standard)</th><th>缺陷等級
(Defect Level)</th></tr>
<tr><td>7</td><td>POL 折痕&分層(The folding and peeled offin polarizer)</td><td>偏光片不可有折痕和分層（脫膠）的現象(The folding and peeled offin polarizer are not acceptable).</td><td>次缺
(Min)</td></tr>
<tr><td>8</td><td>輝度及均勻性、色度(Brightness and uniformity、Chroma)</td><td>應符合規範或圖紙要求規格(Shall be in accordance with the drawings and specification requirements specifications).</td><td>主缺
(Maj)</td></tr>
<tr><td>9</td><td>MURA</td><td>(5% ND Filter)灰階 50%</td><td></td></tr>
</table>

<table>
<tr><td>10</td><td>電性測試（Electrlcal Testing）</td><td>1.顯示缺畫(Missing line character and icon).
2.無功能與無顯示(No function or no display).
3.顯示故障(Display malfunction).
4.LCD 視角缺陷(LCD viewing angle defect).
5.消耗電流超出規格(Current consumption exceeds product specifications).</td><td>主缺
(Maj)</td></tr>
<tr><td>11</td><td>亮點、暗點(Bright dot、Dark dot)On-display
Pixel：3 dot in 1 pixel
  </td><td>
<table>
<tr><th>尺寸
(Size)</th><th>Item</th><th>判定標準(Judging standard)</th><th>允收數量
(Acceptance(Q'ty))</th></tr>
<tr><td rowspan="5">1.44”~
4.9”</td><td rowspan="2">Bright dot</td><td>D≦1/2 Pixel</td><td>忽略不計(Ignore)</td></tr>
<tr><td>1/2 Pixel＜D≦1 Pixel</td><td>N≦1</td></tr>
<tr><td rowspan="2">Dark dot</td><td>D≦1/2 Pixel</td><td>忽略不計(Ignore)</td></tr>
<tr><td>1/2 Pixel＜D≦1 Pixel</td><td>N≦2</td></tr>
<tr><td colspan="2">Total</td><td>N≦3</td></tr>
</table>
distance >=5mm
</td><td>次缺
(Min)</td></tr>
</table>

winstar

LCM Sample Estimate Feedback Sheet

Module Number： _____

1、Panel Specification：

1.	Panel Type：	□ Pass	□ NG ,_____
2.	View Direction：	□ Pass	□ NG ,_____
3.	Numbers of Dots：	□ Pass	□ NG ,_____
4.	View Area：	□ Pass	□ NG ,_____
5.	Active Area：	□ Pass	□ NG ,_____
6.	Operating Temperature：	□ Pass	□ NG ,_____
7.	Storage Temperature：	□ Pass	□ NG ,_____
8.	Others：_____		

2、Mechanical

1.	PCB Size：	□ Pass	□ NG ,_____
2.	Frame Size：	□ Pass	□ NG ,_____
3.	Material of Frame：	□ Pass	□ NG ,_____
4.	Connector Position：	□ Pass	□ NG ,_____
5.	Fix Hole Position：	□ Pass	□ NG ,_____
6.	Backlight Position：	□ Pass	□ NG ,_____
7.	Thickness of PCB：	□ Pass	□ NG ,_____
8.	Height of Frame to PCB：	□ Pass	□ NG ,_____
9.	Height of Module：	□ Pass	□ NG ,_____
10.	Others：	□ Pass	□ NG ,_____

3、Relative Hole Size：

1.	Pitch of Connector：	□ Pass	□ NG ,_____
2.	Hole size of Connector：	□ Pass	□ NG ,_____
3.	Mounting Hole size：	□ Pass	□ NG ,_____
4.	Mounting Hole Type：	□ Pass	□ NG ,_____
5.	Others：	□ Pass	□ NG ,_____

4、Backlight Specification：

1.	B/L Type：	□ Pass	□ NG ,_____
2.	B/L Color：	□ Pass	□ NG ,_____
3.	B/L Driving Voltage (Reference for LED Type)：	□ Pass	□ NG ,_____
4.	B/L Driving Current：	□ Pass	□ NG ,_____
5.	Brightness of B/L：	□ Pass	□ NG ,_____
6.	B/L Solder Method：	□ Pass	□ NG ,_____
7.	Others：	□ Pass	□ NG ,_____

>> **Go to page 2** <<

5、Electronic Characteristics of Module：

1.	Input Voltage：	□ Pass	□ NG ,_____
2.	Supply Current：	□ Pass	□ NG ,_____
3.	Driving Voltage for LCD：	□ Pass	□ NG ,_____
4.	Contrast for LCD：	□ Pass	□ NG ,_____
5.	B/L Driving Method：	□ Pass	□ NG ,_____
6.	Negative Voltage Output：	□ Pass	□ NG ,_____
7.	Interface Function：	□ Pass	□ NG ,_____
8.	LCD Uniformity：	□ Pass	□ NG ,_____
9.	ESD test：	□ Pass	□ NG ,_____
10.	Others：	□ Pass	□ NG ,_____

6、Summary：

Sales signature：_____

Customer Signature：_____ **Date：** / /

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