



Chefree Technology Corp.

TFT COLOR LCD MODULE

MODEL: CH121ILGL-001 (Complied with RoHS)

LVDS interface

Version: P03

Customer :	
Approved By :	
Date:	

	CHEFREE	
APPROVAL	CHECKER	PREPARE
Tim	Mark	Benson



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1. RECORD OF REVISION

Rev	DATE	PAGE	SUMMARY
P01	2016.04.28	ALL	Preliminary specification was first issued.
P02	2016.11.15	ALL	Modify: 2pcs Module 1pcs PP plate;20pcs/carton,
P03	2022.04.05	7	Modify: a.The supply voltage (Min.) of VDD is -0.3V. b.The supply voltage(Max.) of VDD is 4V.
P03	2022.04.05	17	Modify: a.The common mode voltage(Min.) is 0.7V. b.The common mode voltage(Max.) is 1.6V.
P03	2022.04.05	21	Modify: a.The H Total Time(Max) is 1400. b.The V Total Time(Max) is 820.

2.0 General Descriptions

2.1 Introduction

The CH121ILGL-001 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a backlight system, column driver and row driver circuit. This TFT LCD has a 12.1-inch diagonally measured active display area with XGA resolution (1024 horizontal by 768 vertical) pixels arrays.

2.2 Features

- 12.1" TFT LCD Panel
- LED Backlight System
- Supported XGA 1024x768 pixels resolution
- Compatible with RoHS standard

2.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	12.1	Inch
Active Area	245.76 (H) x184 <mark>.32 (V)</mark>	mm
Pixels H x V	1024(RGB) x768	-
Pixel Pitch	0.24(H)×0.2 <mark>4 (</mark> V)	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally White	-
White Luminance	350 (TYP)	cd /m ²
Contrast Ratio	800 (TYP)	-
Response Time	16 (TYP)	msec
Input Voltage	3.3	V
Power Consumption	6.925 (Max)	W
Weight	545 (Max)	g
Outlin <mark>e</mark> Dimension	279.0(H) ×209.0(V) ×9.0(D)	mm
Electr <mark>ic</mark> al Interface (L <mark>o</mark> gic)	LVDS	-
Supp <mark>ort</mark> Color	262K/16. <mark>7</mark> M	-
Optimum Viewing Direction	6 o'cl <mark>oc</mark> k	-
Surface Treatment	Anti-glare & hardness 3H	-



2.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

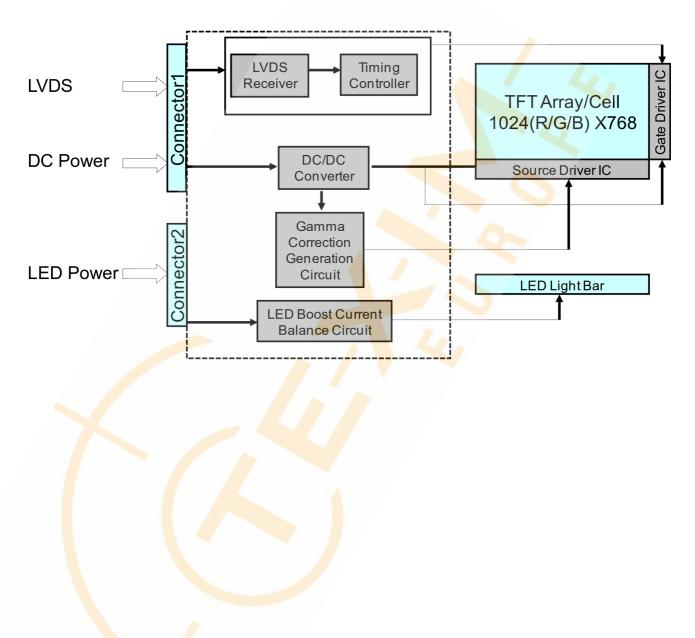
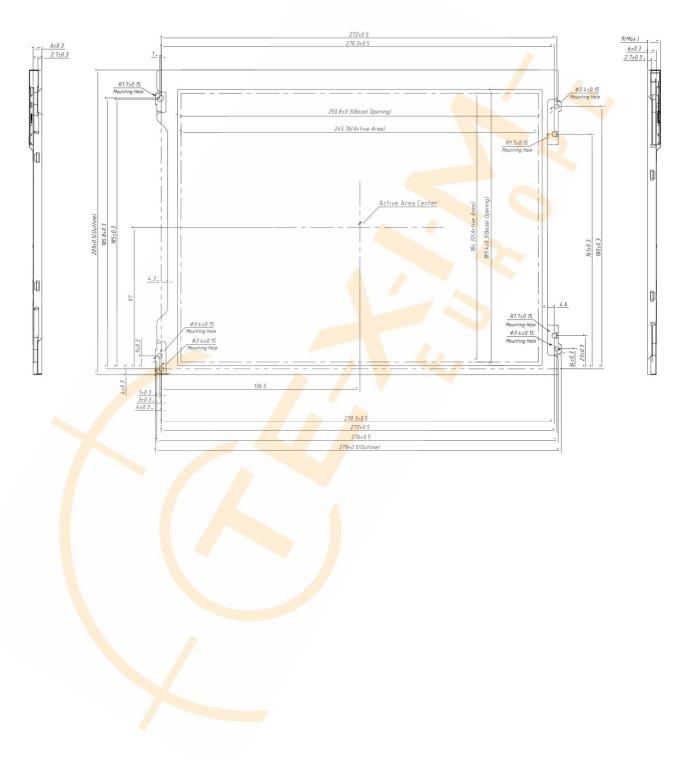


Figure 1 Block Diagram

3.0 Mechanical Characteristics

3.1 Outline Drawing







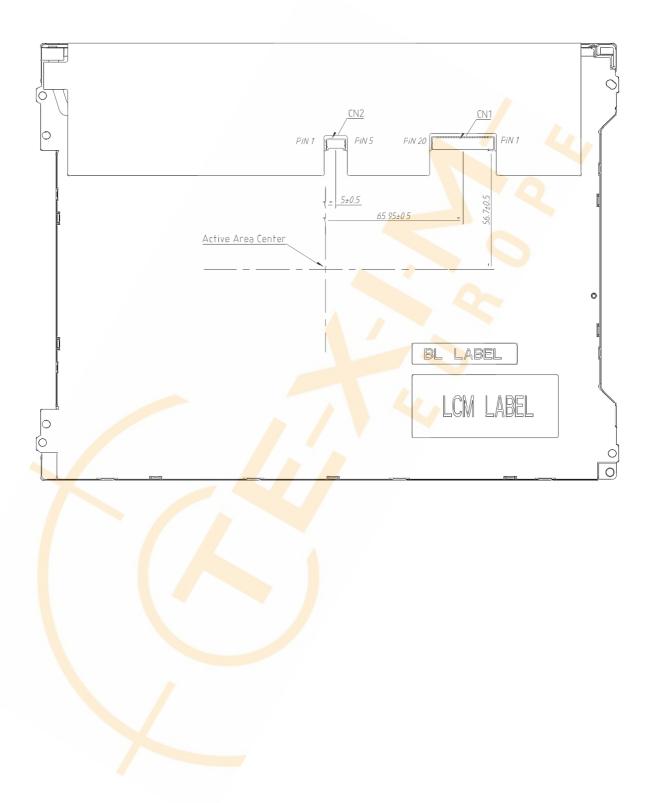
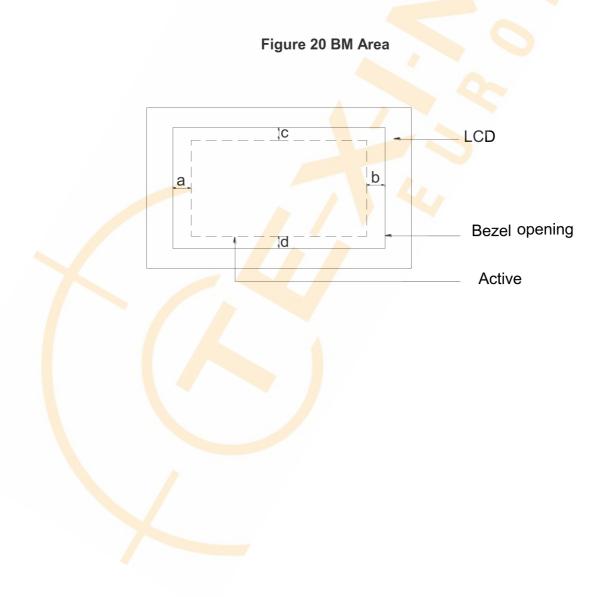


Figure 19 Outline Drawing (Back Side)

3.2 Dimension Specifications

Table 12 Module Dimension Specifications

Item	Min.	Тур.	Max.	Units	
Width	278.5	279.0	279.5	mm	
Height	208.5	209.0	209.5	mm	
Thickness	5.7(without	6(without	6.3(w <mark>it</mark> hout		
	PCBA)	PCBA)	PCBA)	mm	
Weight	-	518.7	545	g	
BM: a-b & c-d		≤1.0		mm	



4.0 Absolute Maximum Ratings

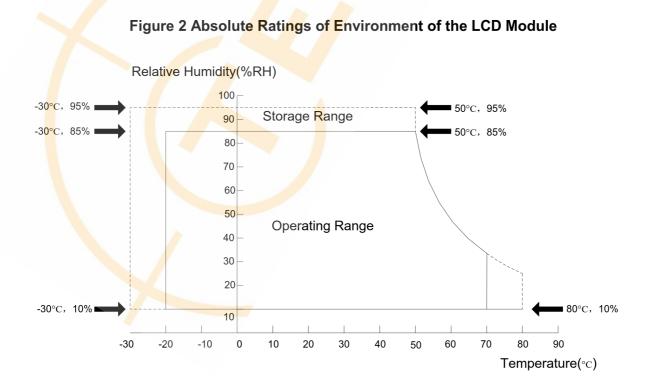
Table 1 Absolute Ratings of Environment							
Item	Symbol	Min.	Max.	Unit	Conditions		
Supply Voltage	V _{DD}	-0.3	4	V	(1)		
Operating Temperature	Тор	-20	70	°C	(1) (2) (3) (4)		
Operating Humidity	Нор	10	85	%RH	-		
Storage Temperature	Тѕт	-30	80	°C	-		
Storage Humidity	Нѕт	10	95	%RH	-		

Table 1 Absolute Ratings of Environment

Note (1): Humidity: 85%RH Max. (T<=40°C) Note static electricity.

Maximum wet bulb temperature at 39° C or less. (T>40°C) No condensation.

- Note (2): There is a possibility of causing deterioration in the irregularity and others of the screen and the display fineness though the liquid crystal module doesn't arrive at destruction when using it at 80~85°C or -20°C.
- Note (3): There is a possibility of causing the fineness deterioration by the prolonged use in the (high temperature) humidity environment (60% or more).
- Note (4): In the operating temperature item, the low temperature side is the ambient temperature regulations. The high temperature side is the panel surface temperature regulations.
- Note (5): Storage Range&Operating Range Picture:



5.0 Pixel Format Image

Figure 1 shows the relationship of the input signals and LCD pixel format image.

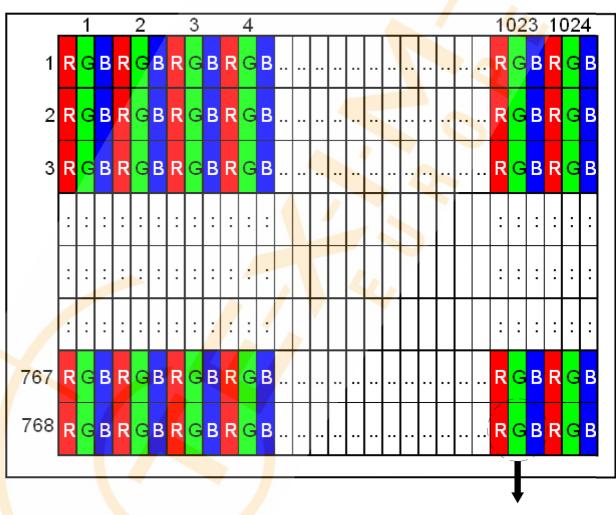


Figure 3 Pixel Format

R Dot +G Dot +B Dot=1 Pixel

6.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

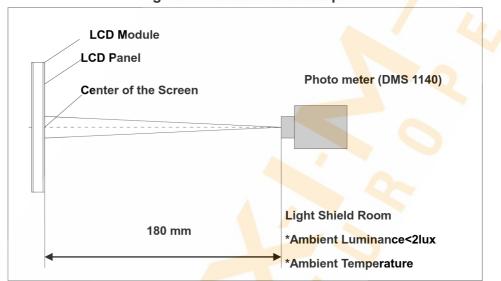
Item	Conditions		Min.	Тур.	Max.	Unit	Note
	Horizontal	θ+	70	80	-		
Viewing Angle	Honzoniai	θ _{x-}	70	80	-		
(CR>10)	Vertical	θ _{y+}	70	80		degree	(1),(2),(3)
	ventical	θ _{y-}	70	80	-		
Contrast Ratio	Center		720	800	-	- 0	(1),(2),(4)
	Rising (90% \rightarrow 1	10%)	-	4	5.2		
Response Time	Falling (10% \rightarrow	90%)	-	12	15.6	ms	(1),(2),(5)
	Rising + Falling	-	16	20.8			
	White x		0.255	0.305	0.355	-	
	White y		0.275	0.325	0.375	-	
	Red x	0.614	0.644	0.674	-		
Color Chromaticity	Red y Green x		0.314	0.344	0.374		-
(CIE1931)			0.280	0.310	0.340	-	(1),(2)
	Green y		0.604	0.634	0.664	-	
	Blue x		0.122	0.152	0.182	-	
	Blue y		0.051	0.081	0.111	-	
NTSC		-	72	-	-		
White Luminance	5 Points Average		<mark>3</mark> 15	350	-	cd/m^2	(1),(2),(6)
Lumin <mark>an</mark> ce Unifor <mark>m</mark> ity	9 Points		75	80	-	%	(1),(2),(7)

Table 2 Optical Characteristics



Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature (25° C) for 15 minutes to Avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



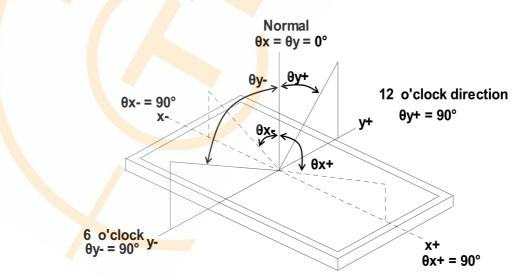


Note (2) The LED input parameter setting as: I_LED: 240mA

V_LED: 12V PWM_LED: Duty 100%

Note (3) Definition of Viewing Angle



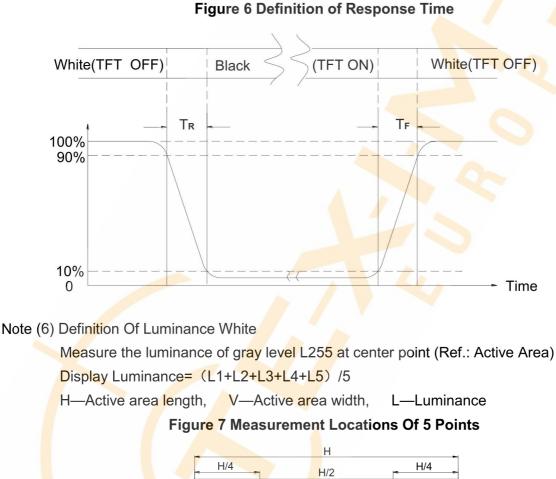


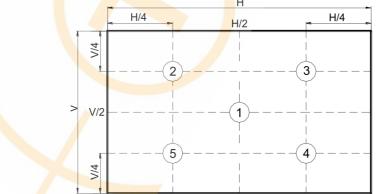


Note (4) Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression Contrast Ratio (CR) = L255/ L0 L255: Luminance of gray level L255, L0: Luminance of gray level 0

Note (5) Definition Of Response Time (T_R, T_F)





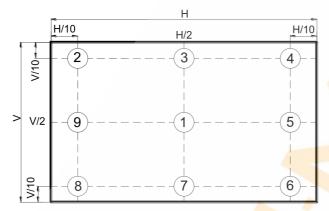
Note (7) Definition Of Luminance Uniformity (Ref.: Active Area)



Measure the luminance of gray level 255 at 9 points.

 $\text{UNF(9pts)} = \frac{\text{Min}(L1, L2, \Lambda L9)}{\text{Max}(L1, L2, \Lambda L9)}$

Figure 8 Measurement Locations of 9 Points



7.0 Backlight Characteristics

5.1 Parameter Guideline Of LED Backlight

Table 3 Parameter Guideline for LED Backlight

ltem	Symbol		Min.	Тур.	Max.	Units	Note
LED Input Voltage	V_led		10.8	12	12.6	V	(2)
LED Power Consumption	P_led		-	-	6.1	W	(2)
LED Forward Voltage	V _F		2.8	3.3	3.6	V	4
LED Forward Current	I _F		-	60	-	m A	
DW/M Signal Valtage	V _{PWM_EN}	High	4.5	5	5. <mark>5</mark>	V	(2)
PWM Signal Voltage		Low	0	-	0.5		
LED Enable Voltage	V _{LED_EN}	High	2.0	5	5.5	V	
		Low	-	0	0.5		
Input PWM Frequency	FPWM		200	-	20,000	Hz	
LED Life Time	LT		30,000	-	-	Hours	(1)(2)
Duty Ratio	PWM		5	-	100	%	(2)

Note (1) The LED life time define as the estimated time to 50% degradation of initial luminous.

Note (2) Operating temperature 25°C, humidity 55%RH.

Table 4 Connector Name / Designation

Item	Description				
Input LED	PCB Jack Connector model: MSB24038P5A				
	Manufactured by STM				
	PIN IDE Connector model: P24038P5				

Table 5 Input LED Signal Pin Assignment

Pin #	Function
1	VCC(12V input)
2	GND
3	On/Off(5V-ON,0V-OFF)
4	Dimming(PWM)
5	NC

8.0 Electrical Characteristics

8.1 Interface Connector

Table 6 Connector Name / Designation

Item	Description			
FPC Down Connector	PCB Jack Connector recommended model: MSB240420HE			
(20pin pitch=1.25mm)	Manufactured by STM			
	PIN IDE Connector model: P240420H			

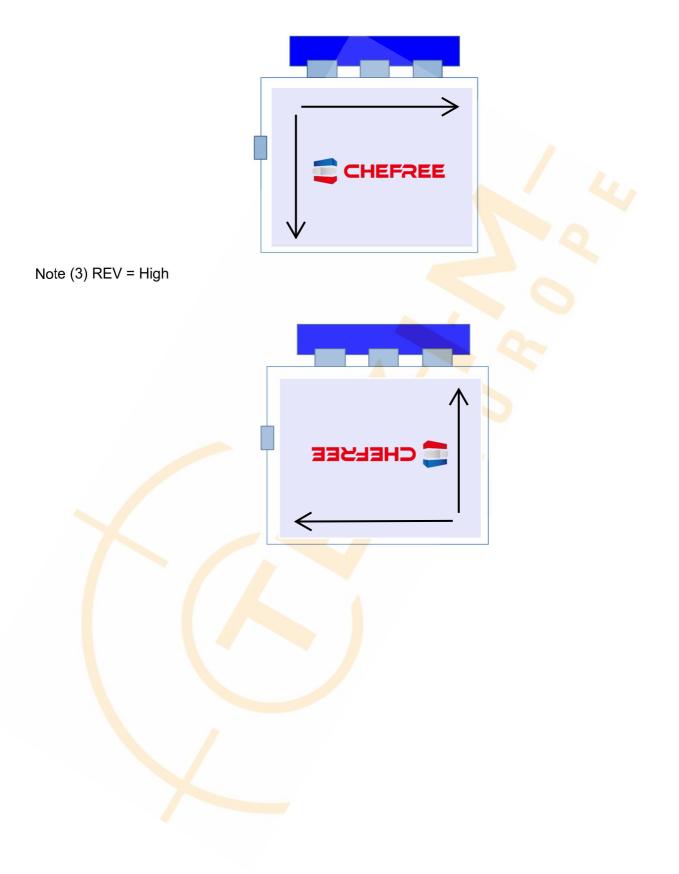
Din #	Cumph of	Description				
Pin #	Symbol	Description				
1	VDD	Power Supply, 3.3V (typical)				
2	VDD	Power Supply, 3.3V (typical)				
3	VSS	Ground				
4 REV		Reverse Scan selection				
4	REV	{High:2.5(min), 3.3(ty <mark>p),</mark> 3.6(max); Low: 0.5(max)}				
5	Rin1-	-LVDS differential data input (R0-R5,G0)				
6	Rin1+	+LVDS differential data input (R0-R5,G0)				
7	VSS	Ground				
8	Rin2-	-LVDS di <mark>ffer</mark> ential data input (G1-G5, B0-B1)				
9	Rin2+	+LVD <mark>S di</mark> ffer <mark>ent</mark> ial d <mark>ata</mark> input (G1-G5,B0-B1)				
10	VSS	Ground				
11	Rin3-	-LVDS differential data input (B2-B5,HS,VS,DE)				
12	Rin3+	+LVDS differential data input (B2-B5,HS,VS,DE)				
13	VSS	Ground				
14	CikiN-	-LVDS differential clock input				
15	ClkIN+	+LVDS differential clock input				
16	GND	Ground				
17	Rin4-	-LVDS differential data input (R6-R7,G6-G7,B6-B7)				
18	Rin4+	+VDS differential data input (R6-R7,G6-G7,B6-B7)				
19	SEL68	6/8 bits LVDS data input selection(H:8bit L/NC:6bit)				
20	Bist	Internal use				

Table 7 Signal Pin Assignment

Note(1) : All input signals shall be low or Hi-resistance state when VDD is off.

Note (2) REV = LOW/NC





6.2 LVDS Receiver

6.2.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Differential Input High Threshold	Vth	-		+100	mV	V _{CM} =+1.2V
Differential Input Low Threshold	Vtl	-100	-	-	mV	V _{CM} =+1.2V
Magnitude Differential Input Voltage	V _{ID}	100	-	600	mV	-
Common Mode Voltage	V _{CM}	0.7	-	1.6	V	-
Common Mode Voltage Offset	ΔV_{CM}	-	-	50	mV	V _{CM} =+1.2V

Table 8 LVDS Receiver Electrical Characteristics

Note: (1) Input signals shall be low or Hi- resistance state when VDD is off.

(2) All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.



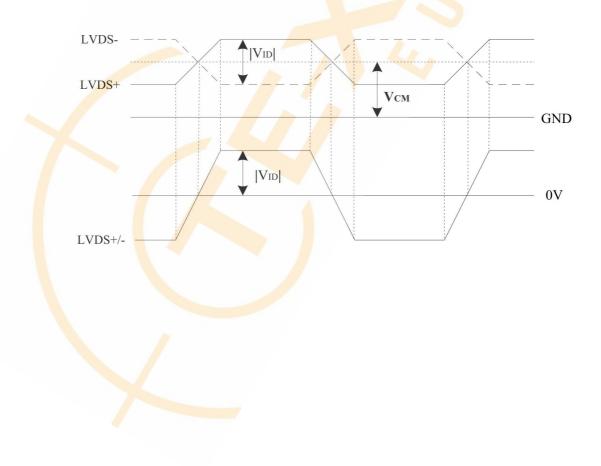
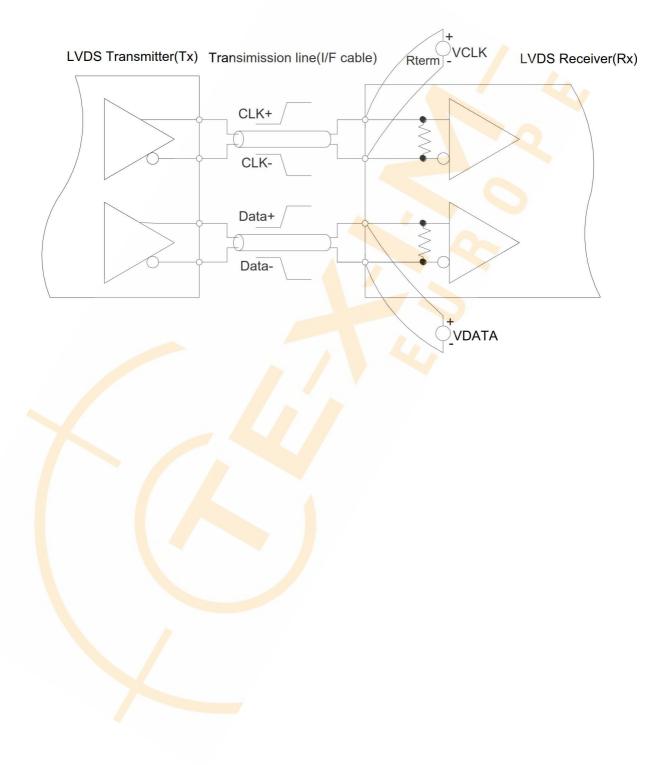
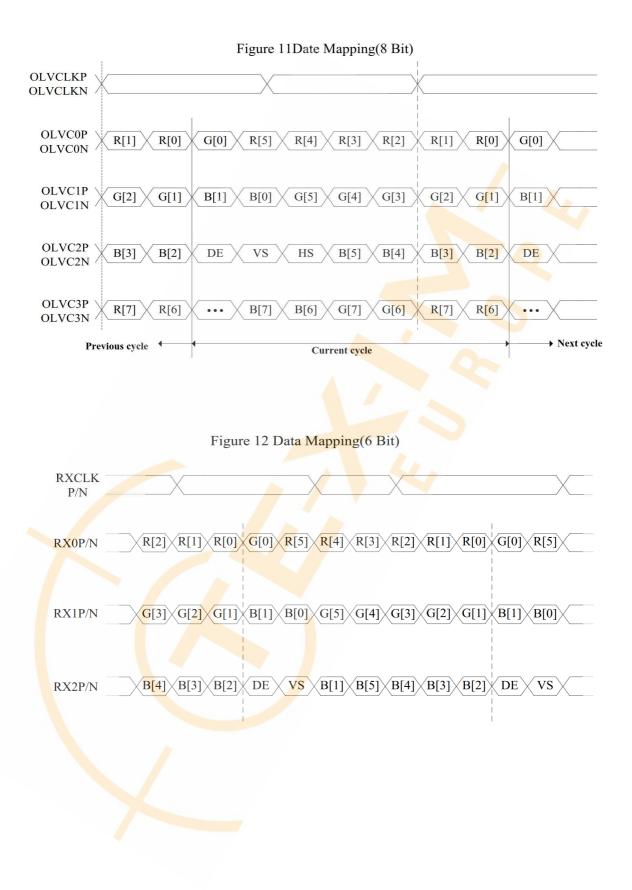




Figure10 Measurement System







8.2.2 LVDS Receiver Internal Circuit

Figure 13 LVDS Receiver Internal **Circuit** shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

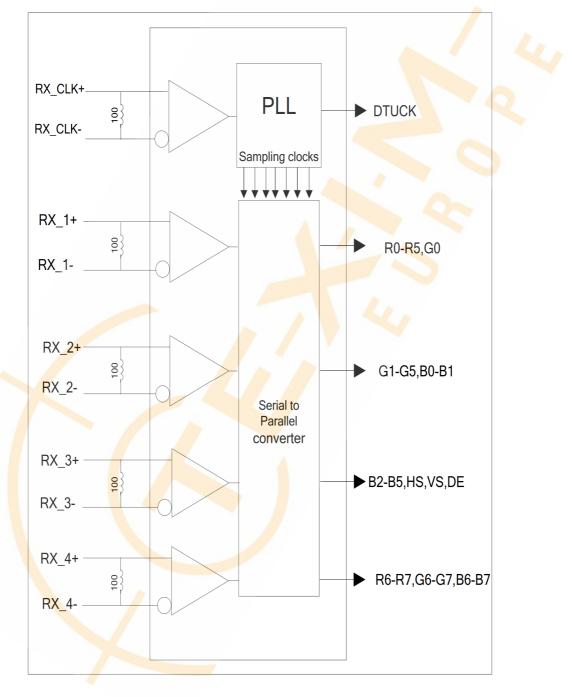


Figure 13 LVDS Receiver Internal Circuit

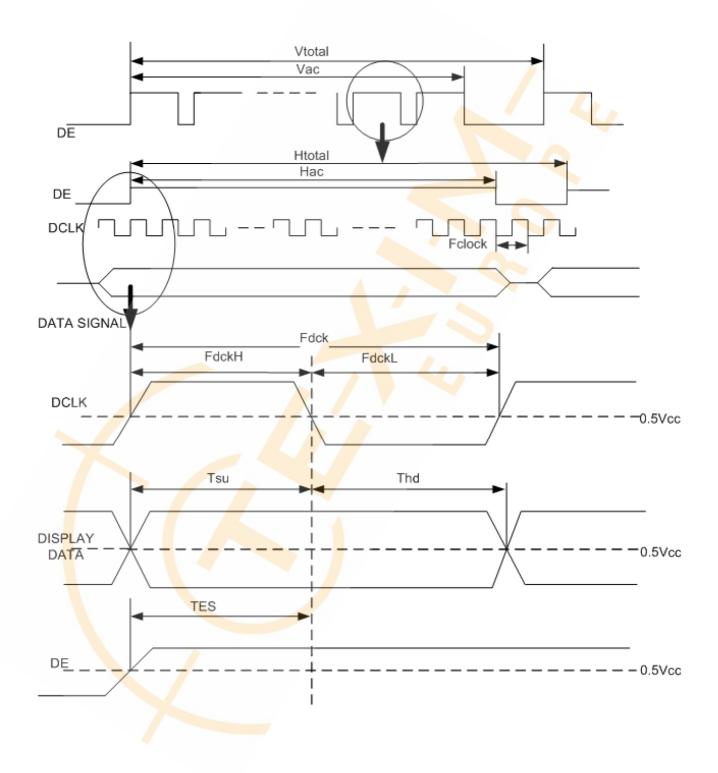
9.0 Interface Timings

Table 9 Interface Timings								
Parameter	Symbol	Unit	Min.	Тур.	Max.			
LVDS Clock Frequency	Fclk	MHz	50	65	80			
H Total Time	HT	Clocks	1100	1344	1400			
H Active Time	HA	Clocks	1024	1024	1024			
H Blanking Time	HBL	Clocks	76	320	1023			
V Total Time	VT	Lines	776	806	820			
V Active Time	VA	Lines	7 <mark>68</mark>	768	768			
V Blanking Time	VBL	Lines	8	38	255			
Frame Rate	Vsync	Hz	55	60	65			

Note: H Blanking Time and V Blanking Time can not be changed at every frame.



Figure 14 Timing Characteristics



10.0 Power Consumption

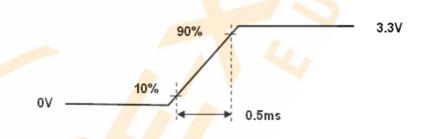
Input power voltage specifications are as follows.

Item		Symbol	Min.	Тур.	Max.	Units	Note
LCD Drive Voltage (Logic)		VDD	3.0	3.3	3.6	V	(2), (4)
VDD Current	Black Pattern	IDD	-	-	250	mA	
VDD Power Consumption	Black Pattern	PDD	-	-	0.825	W	(3),(4),(6)
Rush Current		Irush	-	-	3	А	(1),(4),(5)
Allowable Logic/LCD Drive Ripple Voltage		VDDrp	-	-	200	mV	(4)

Table 10 Power Voltage

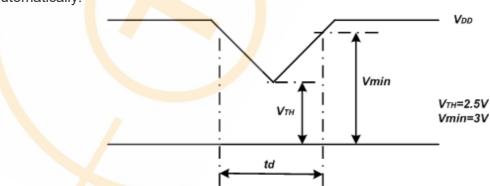
Note (1) Measure Condition





Note (2) VDD Power Dip Condition

If VTH<VDD≤Vmin, then td≤10ms; When the voltage returns to normal our panel must revive automatically.



Note (3) Frame Rate=60Hz, VDD=3.3V,DC Current.

Note (4) Operating temperature 25 $^\circ\! \mathbb{C}$, humidity 55%RH.

11.0 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-resistance state or low level when VDD is off.

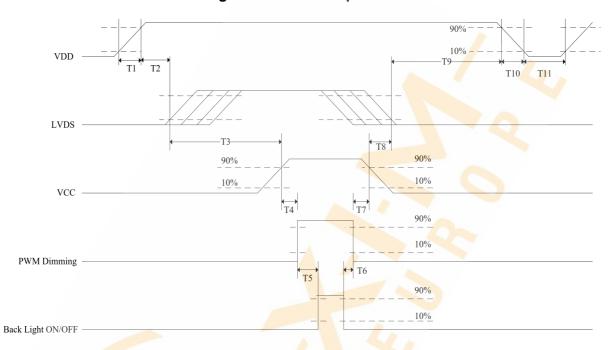


Figure 17 Power Sequence

Parameter	Unit	min	typ	max		
T1	ms	0.5	-	10		
T2	ms	30	40	50		
T3	ms	200	-	-		
T4	ms	10	-	-		
T5	ms	10	-	-		
T6	ms	0	-	-		
T7	ms	10	-	-		
T 8	ms	100	-	-		
Т9	ms	0	16	50		
T10	ms	-	-	10		
T11	ms	1000	-	-		

Table 11 Power Sequencing Requirements

Note (1) Power On Sequence: VCC-> AVDD -> VGL -> VGH -> Data -> B/L

(2) Power Off Sequence: B/L-> Data -> VGH -> VGL -> AVDD -> VCC

12.0 Reliability Conditions

ltem	Package	Test Conditions	Note
High Temperature Operation Test	Module	70℃, 300hrs	1,2,3,4,5,6
Low Temperature Operating Test	Module	-20 °C , 300hrs	1,2,3,4,5,6
High Temperature Storage Test	Module	80℃, 300hrs	1,3,4,5,6
Low Temperature Storage Test	Module	-30°C , 300hrs	1,3,4,5,6
High Temp High Humidity Operating Test	Module	50℃, 85<mark>%, 300</mark>hrs	1,2,3,4,5,6

Note:

- 1. There is no function defect and occurrence of any new defective shall not be allowed.
- 2. In Operating test, the B/L voltage and current must be in spec.
- 3. All the judgments are under normal temperature and the sample need to be static more than 2 hours in the normal temperature before judge.
- 4. During measurement, the condensation water or remains shall not be allowed.
- 5. The minimum sample quantity of test is 3pcs.
- 6. There is no display function fail issue occurred, all the cosmetic specification is judged before the reliability stress.

13.0 General Precaution

13.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

13.2 Handling Precaution

- (1) Please mount LCD module by using mounting holes arranged in four corners tightly.
- (2) Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. CHEFREE does not warrant the module, if customers disassemble or modify the module.
- (3) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid Crystal, and do not contact liquid crystal with skin. If liquid crystal contacts mouth or eyes, rinse out with water immediately. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and Rinse thoroughly with water.
- (4) Disconnect power supply before handling LCD module
- (5) Refrain from strong mechanical shock and /or any force to the module.
- (6) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature; etc otherwise LCD module may be damaged. It's recommended employing protection circuit for power supply.
- (7) Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when Persons handle the LCD module for incoming inspection or assembly.
- (8) When the surface is dusty, please wipe gently with absorbent cotton or other soft Material. When cleaning the adhesives, please use absorbent cotton wetted with a little Petroleum benzene or other adequate solvent.
- (9) Wipe off saliva or water drops as soon as possible. If saliva or water drops Contact with polarizer for a long time, they may causes deformation or color Fading.
- (10) Protection film must remove very slowly from the surface of LCD module to Prevent from electrostatic occurrence.
- (11) Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is Very weak to electrostatic discharge, Please be careful with electrostatic Discharge .Persons who handle the module should be grounded through adequate methods.
- (12) Do not adjust the variable resistor located on the module.

13.3 Storage Precaution

- (1) Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
- (2) The module shall not be exposed under strong light such as direct sunlight.Otherwise, Display characteristics may be changed.
- (3) The module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.

13.4 Operation Precaution

- (1) Do not connect or disconnect the module in the "Power On" condition.
- (2) Power supply should always be turned on/off by "Power on/off sequence"
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding



methods may be important to minimize the interference.

(4) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

13.5 Others

- (1) Ultra-violet ray filter is necessary for outdoor operation.
- (2) Avoid condensation of water which may result in improper operation or disconnection of electrode.
- (3) If the module keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.
- (4) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

13.6 Disposal

When disposing LCD module, obey the local environmental regulations.

