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TFT DISPLAY SPECIFICATION



WINSTAR Display Co.,Ltd. 華凌光電股份有限公司





SPECIFICATION

CUSTOMER :

MODULE NO.: WF1560ATWFA5LENO#

APPROVED BY:		N ⁻ E
(FOR CUSTOMER USE ONLY)		OP E
	PCB VERSION:	DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
			葉虹蘭
ISSUED DATE:	2023/11/08		

TFT Display Inspection Specification: <u>https://www.winstar.com.tw/technology/download.html</u> Precaution in use of TFT module: <u>https://www.winstar.com.tw/technology/download/declaration.html</u>

Winstar Display Co., LTD 華凌光電股份有限公司				MODLE NO :
REC	ORDS OF REV	ISION	DOC. FIRST ISSUE	
VERSION	DATE	REVISED PAGE NO.	SU	MMARY
0	2023/11/08		Fi	rst issue



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1.Module Classification Information

W	F	1560	А	Т	W	F	A5	L	Е	Ν	0	#
(1)	2	3	4	(5)	6	$\overline{\mathcal{I}}$	8	9	10	(1)	(12)	(13)

1) Brand : WINSTAR DISPLAY CORPORATION													
2	Disp	lay Type:F	`→]	ГГТ Туре	e, J—	>Cu	stom TF	T						
3	Disp	lay Size:1:	5.6"	TFT										
4	Mod	el serials no	•											
6	Back	light	F-	→CCFL,	Wh	ite				$T \rightarrow LED$,	Whi	te		
	Туре	;:	S-	→LED, H	Iigh	Lig	ht White	•		Z→Nichi	a LE	D, White		
		Doloriza	A-	→Transn	nissi	ve, l	N.T, IPS	TF	Т	Q→Trans	miss	ive, Super V	W.T,	12:00
	Tung		C-	→Transn	nissi	ve, l	N. T, 6:0	0;		R→Trans	miss	ive, Super V	W.T, 9	O-TFT
	Tem	nerature	F-	→Transm	nissiv	ve, N	N.T,12:0	0;		V→Trans	miss	ive, Super V	W.T,	VA TFT
6	rong	o Grav	I—	>Transm	issiv	ve, W	V. T, 6:0	0		W→Trans	smiss	sive, Super	W.T,	IPS TFT
	Soal	- Unay	K-	→Transf	lecti	ve, V	W.T,12:(00		X→Trans	miss	ive, W.T, V	ATF	Т
	Dira	otion	L-	→Transn	nissi	ve, V	W.T,12:0	00		Y→Trans	miss	ive, W.T, II	PS TF	Τ
	Dire	ction	N-	→Transn	nissi	ve, S	Super W	Υ.Τ, (5:00	Z→Trans	miss	ive, W.T, O	-TFT	
	A : '	TFT LCD								F : TFT+	CON	TROL B	OAR	D
	B:	IFT+SCREV	WE	IOLES+	CON	ITR	OL BOA	ARD)	G: TFT+	- SCI	REW HOLI	ES	
Ø	C:	ΓFT+ SCRE	W I	HOLES -	⊦A/I) BC	DARD			H: TFT+	- <mark>D/</mark> V	BOARD		
	D:T	TFT+ SCREW	HO	LES +A/D	BOA	ARD	+CONTR	OL E	BOAR	D I : TFT+	SCR (EW <mark>H</mark> OLE	S +D	/V BOARD
	$E: \mathbb{I}$	ΓFT+ SC <mark>R</mark> E	WI	HOLES -	-PO	WE]	R BOA	ARD		J: TFT+I	POW	ER BD		
	Reso	olution:												
	Μ	1024 <mark>7</mark> 68	N	12812	28	Р	128 <mark>08</mark>	00	Q	480800	R	640320	S	480128
8	Т	8003 <mark>2</mark> 0	U	8 <mark>0</mark> 012	80	V	176 <mark>2</mark> 2	20	W	1280398	Χ	1024250	Y	1920720
	A5	19201 <mark>0</mark> 80	A6	4804	80	A7	108019	920	A8	135240	A9	480640	B2	122250
	B3	340800	B4	28014	24	B 5	12001	920	B6	4801280	B7	800800	B8	40160
9	Γ): Digital		L:LVDS	5		M:MIP	[E:eDP				
	Inter	face:												
10	Ν	Without co	ontr	ol board	A		8Bit	B		16Bit	Е	eDP	Η	HDMI
	Ι	I2C Ir	ter	face	R	2	RS232	S	S	PI Interface	U	USB		
	TS:													
	Ν	Without TS				Т	Resistiv	e to	uch p	anel C C	Capa	citive touch	pane	el (G-F-F)
(11)	G	Capacitive t	ouc	h panel (G-G)			C1	Capacitive	touc	ch panel (G	-F-F)	+OCA
	C2	Capacitive t	ouc	h panel (G-F	-F)+	OCR		Gl	Capacitive	e touc	ch panel (G	-G)+	OCA
	G2	Capacitive t	ouc	h panel (G-G)+O	CR		В	CTP+GG+	USE	3		
12	Vers	sion:	X:R	aspberry	pi		V: I	Rasp	berry	pi 3B+				
(13)	Spec	ial Code		#:Fit in	with	RO	HS dire	ctive	e regu	lations				

2.Summary

WF1560A is a 15.6" TFT Liquid Crystal Display module with WLED Backlight unit and 30 pins eDP interface (The original TFT panel is 2ch-LVDS). This module supports 1920 x 1080 FHD AAS mode and can display 16,194,277 colors.



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3.General Specifications

ltem	Dimension	Unit
Size	15.6	inch
Dot Matrix	1920 x RGB x 1080	dots
Module dimension	363.8(W) x 215.9(H)x 20.8 (D)	mm
Active area	344.16 x 193.59	mm
Pixel pitch	0.17925 (H) x 0.17925 (V)	mm
LCD type	TFT, Normally Black, Transmissive	
Viewing Angle	89/89/89/89	
Backlight Type	LED,Normally White	
Controller IC	CH7513A-BFI	
TFT Interface	eDP	
With /Without TP	Without TP	P
Surface	Anti-Glare	

*Color tone slight changed by temperature and driving voltage.

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4.Absolute Maximum Ratings

ltem	Symbol	Min	Тур	Max	Unit
Operating Temperature	TOP	-30	_	+85	°C
Storage Temperature	TST	-40	_	+90	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. $\leq 60^{\circ}$ C, 90% RH MAX. Temp. > 60°C, Absolute humidity shall be less than 90% RH at 60°C



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5.Electrical Characteristics

5.1. Operating conditions:

ltem	Symbol	Min	Тур	Мах	Unit	Remark
Supply Voltage For LCM	P1 VDD	4.7	5	5.3	V	-
Supply Current For LCM	P1 IDD	_	900	1350	mA	Note 1,2

5.2. Backlight conditions:

ltem	Symbol	Min	Тур	Мах	Unit	Remark
Supply Voltage For Back Light	P2 VDD	11.5	12	12.5	V	-
Supply Current For Back Light	P2 IDD	_	1000	1500	mA	Note 1,2
LED life time	_	_	50,000	_	Hr	Note 3

Note 1 : This value is test for P1 VDD=5.0V , P2 VDD =12.0V , Ta=25 $^\circ C$ only

Note 2 : Please make sure to support enough current.

Note 3: The "LED life time" is defined as the module brightness decrease to 50% original

brightness at Ta=25°C

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5.3. Signal Electrical Characteristics

Input signals shall be low or High-impedance state when P1 VDD is off. It is recommended to refer the specifications of VESA Display Port Standard V1.2 in detail.

Parameter	Description	Min.	Тур.	Max.	Unit	
V _{CM}	Differentia Common Mode Voltage	0	-	2.0	V	
V _{Diff P-P} Level 1 Differential Peak to Peak Voltage Level 1		0.34	0.40	0.46	V	
V _{Diff P-P} Level 2 Differential Peak to Peak Voltage Level 2		0.51	0.60	0.68	V	
Vdiff P-P Level 3	Differential Peak to Peak Voltage Level 3	0.69	0.80	0.92	V	
VDiff P-P Level 4	Differential Peak to Peak Voltage Level 4	1.02	1.20	1.38	V	

Table 1 Display Port Main Link

Note: Fallow as VESA display port standard V1.2 at both 1.62 and 2.7Gbps link rates.

Figure 2 Display Port Main Link Signal

Figure 3 Display Port AUX_CH Signal



Table 2 Display Port AUX_CH

Parameter	Description	Min.	Тур.	Max.	Unit
Vсм	Differentia Common Mode Voltage	0	VDD/2	2	V
VDiff P-P	Differential Peak to Peak Voltage	0.39	Ð	1.38	V

Note: Fallow as VESA display port standard V1.2.

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Table 3 Display Port VHPD

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Table 4 eDP	Panel	Power	Sequence	Timing	Parameters
-------------	-------	-------	----------	--------	------------

Timing	Description	Reqd.	Lin	nits	Notes
rarameter		U,	Min.	Max.	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	• 1
Т2	Delay from LCD VCC to black video generation	Sink	Oms	200ms	Prevents display noise until valid video data is received from the Source.(see note 1 below)
тз	Delay from LCD VCC to HPD high	Sink	Oms	200ms	Sink Aux Channel must be operational upon HPD high.
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize.
T5	Link training duration	Source	-		Dependant on Source link training protocol.
T6	Link idle	Source	-		Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
77	Delay from valid video data from Source to video on display	Sink	Oms	50ms	Max allows Sink validate video data and timing.
Т8	Delay from valid video from Source to backlight enable	Source			Source must assure display video is stable.
Т9	Delay from backlight disable to end of valid video data	Source		ñ	Source must assure backlight is no longer illuminated.(see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	Oms	500ms	
T 11	Power rail fall time, 90% to 10%	Source	270	10ms	
T12	Power off time	Source	500ms	÷	-

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Note 1: The Sink must include the ability to generate black video autonomously. The Sink must automatically enable black video under the following conditions:

- Upon P1 VDD power-on (within T2 max)

- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

- When no Main Link data, or invalid video data, is received from the Source. Black video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The Sink may implement the ability to disable the black video function, as described in Notes 1, above, for system development and debugging purposes.

Note 3: The Sink must support Aux Channel polling by the Source immediately following P1 VDD power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready).

The Sink must be able to respond to an Aux Channel transaction with the time specified within T3max.



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6.Pixel Format Image

Figure 6 shows the relationship of the input signals and LCD pixels format image. Figure 6 Pixel Format

33	1			2			3	7 -		1	31	10	70			19	19		19	20		
1	R	G		R	G		R	G			•••					R	G		R	G		
2	R	G	B	R	G		R	G		• •	•••	••••		••••		R	G		R	G		
3	R	G		R	G		R	G			•••					R	G		R	G		
4	R	G		R	G		R	G								R	G		R	G		
5	R	G		R	G		R	G		•••	•••	• •		•••		R	G		R	G		
	:	200	÷	•		:		:	:									20		1000	<u>)</u>	
	:		:		•••	:	·	·	:							•		÷	1.00	•		
	•	•				:	:		:												<u>)</u>	
	3		:	•••	••				:									:		342	1.18	
	:	•	:	:	:	:		:	:						E							
1079	R	G	B	Ř	G	B	R	G	d							R	G	в	R	G	B	
1080	R	G	в	R	G		R	G								R	G		R	G		

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7.Interface Timings

7.1. Timing Characteristics

Basically, interface timings should match the 1920 x 1080 /60Hz manufacturing guide line timing.

Table Interface Timings

The input signal timing (2ch-LVDS) specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
	Frequency	Fc	60	70.93	75	MHz	-
	Period	Tc		14.1		ns	-
	Input cycle to cycle jitter	T _{rcl}	-0.02*Tc		0.02*Tc	ns	-
	Input clock to data skew	TLVCCS	-0.02*Tc		0.02*Tc	ns	-
2ch-LVDS Clock	Spread spectrum modulation range	Fclkin_ mod	FC*98%		FC*102%	MHz	
	Spread spectrum modulation frequency	F _{SSM}			200	KHz	-
	Frame Rate	Fr	50	60	60	Hz	Tv=Tvd+Tvb
	Total	Tv	1090	1110	1130	Th	-
Vertical Display Term	Active Display	Tvd	1080	1080	1080	Th	
	Blank	Tvb	Tv-Tvd	30	Tv-Tvd	Th	
	Total	Th	1050	1065	1075	Tc	Th=Thd+Thb
Horizontal Display Term	Active Display	Thd	960	960	960	Тс	-
	Blank	Thb	Th-Thd	105	Th-Thd	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals are ignored.

Note (2) The Tv(Tvd+Tvb) must be integer, otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM





Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T1 – TI

8.Power ON/OFF Sequence

P1/P2 VDD power on/off sequence is as follows. Interface signals are also shown in the chart.Signals from any system shall be Hi-Z state or low level when P1 VDD is off.



Parameter	Unit	Min.	Max.
T1	ms	0.5	10
T2	ms	0	10
Т3	ms	0	200
T4	ms	0	50
Т5	ms	300	9 9 1
Т6	ms	200	
T7	ms	0.5	10
Т8	ms	0	10
Т9	ms	500	-

Table 8-2 Power Sequencing Requirements

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9.Optical Characteristics

ltem		Symbol	Condition.	Min	Тур.	Max.	Unit	Remark	
Response	time	Tr+ Tf	θ=0° 、Φ=0°	-	25	35	.ms	Note 3	
Contrast ratio		CR	At optimized viewing angle	600	800	-	-	Note 4,	
Color	\//bito	Wx	θ-0° 、	0.263	0.313	0.363		Noto 2.6.7	
Chromaticity	vvnite	Wy	θ=0 Φ=0	0.279	0.329	0.379			
	Hor	ΘR		85	89	-		Note 1	
Viewing	Hor.	ΘL		85	89	-	Deg.		
angle	Mar	ФТ	CR <u>≥</u> 10	85	89	-			
	ver.	ФВ		85	89	-			
Brightness		-	-	360	450	-	cd/m ²	Center of display	
Uniformi	ty	(U)	-	70	-	-	%	Note 5	

Ta=25±2°C

Note 1: Definition of viewing angle range



Fig 9.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.



Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed

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from 90% to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10% to 90%



Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

Contrast ratio (CR) = Luminance measured when LCD on the "White" state Luminance measured when LCD on the "Black" state

Note 5: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/Lmax x100%

L = Active area length

W = Active area width



Fig 9.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931) Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

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10.Interface

10.1. CON2 : LCM PIN Definition

Pin No.	Signal Name	Description	Remarks
1	NC	Not connection	
2	GND	Ground	
3	DP1-	Complement Signal Link Lane 1	
4	DP1+	True Signal Line 1	
5	GND	Ground	
6	DP0-	Complement Signal Link Lane 0	
7	DP0+	True Signal Line 0	
8	GND	Ground	
9	AUX+	True Signal Auxiliary Ch.	
10	AUX-	Complement Signal Auxiliary Ch.	
11	GND	Ground	
12-14	NC	Not connection (If Pin 12 and Pin 13 have voltage input, it will not affect the use)	
15-16	GND	Ground	
17	HPD	HPD Signal Pin	F
18-21	GND	Ground	2 4
22	NC(BL_EN)	Not connection	
23	NC(BL_PWM)	C(BL_PWM) Not connection	
24-30	NC Not connection(If Pin 26~Pin 29 have voltage input, it will not affect the use)		

Note: All input signals shall be low or Hi-Z state when P1 VDD is off

10.2. CON3 : Back light PIN Definition

Pin No.	Signal Name	Description	Remarks
1	GND	Ground	
2	BL_EN	Back light Enable	
3	BL_UP	Back light Increment Backlight Brightness	
4	BL_DN	Back light Decrement Backlight Brightness	

Note:

1. An on-screen display (OSD) ,the internal control of brightness will need to switch CON3 to Pin3~Pin4.

2. 100% brightness is preset and the adjustable range will be 0~100%(16 steps)

3. After adjusting the brightness, the brightness will be automatically memorized after 10 seconds.

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Pin No.	Signal Name	Description	Remarks					
1	5V	Power supply +5V						
2	GND	Ground						
3	NC	Not connection						

10.3. P1 : Supply Voltage For LCM

10.4. P2 : Supply Voltage For Back Light

Pin No.	Signal Name	Description	Remarks
1	12V	Power supply +12V	
2	GND	Ground	
3	NC	Not connection	



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11.Block Diagram



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12.Reliability

Content of Reliability Test (Super Wide temperature, -30°C~85°C)

Environmental Tes	t		
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	90°C 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-40°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85°C 200hrs	
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30°C 200hrs	1
High Temperature/ Humidity storage	The module should be allowed to stand at 60°C,90%RH max	60°C,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -30°C 25°C 85°C 	-30°C/85°C 10 cycles	
Vibration te <mark>s</mark> t	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact), ±800v(air), RS=330Ω CS=150pF 10 times	

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

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13.Contour Drawing







LCM Sample Estimate Feedback Sheet

Module Number :		Page: 1
1 · <u>Panel Specification</u> :		
1. Panel Type:	Pass	🗆 NG ,
2. View Direction :	Pass	🗆 NG ,
3. Numbers of Dots :	Pass	🗆 NG ,
4. View Area:	Pass	🗆 NG ,
5. Active Area :	Pass	🗆 NG ,
6. Operating	Pass	🗆 NG ,
7. Storage Temperature :	Pass	🗆 NG ,
8. Others :		
2 <u>Mechanical</u>		
1. PCB Size :	Pass	🗆 NG ,
2. Frame Size :	Pass	🗆 NG ,
3. Material of Frame :	Pass	🗆 NG ,
4. Connector Position :	Pass	🗆 NG ,
5. Fix Hole Position:	□ Pass	🗆 NG ,
6. Backlight Position :	□ Pass	🗆 NG ,
7. Thickness of PCB:	□ Pass	🗆 NG ,
8. Height of Frame to	Pass	🗆 NG ,
9. Height of Module :	□ Pass	□ NG ,
10. Oth <mark>e</mark> rs :	Pass	🗖 🛛 NG , 📶 📃
3 ∖ <u>Relat<mark>iv</mark>e Hole Size</u> :		
1. Pitc <mark>h</mark> of Connec <mark>to</mark> r ∹	D Pass	□ NG ,
2. Hole size of Connector :	□ Pass	□ NG ,
3. Mounting Hole size:	□ Pass	□ NG ,
4. Mounting Hole Type:	□ Pass	□ NG ,
5. Others :	□ Pass	□ NG ,
4 <u> Backlight Specification</u> :		
1. B/L Type ∶	□ Pass	□ NG ,
2. B/L Color :	□ Pass	□ NG ,
3. B/L Driving Voltage (Refer	ence for LED	□ Pass □ NG ,
4. B/L Driving Current :	□ Pass	□ NG ,
5. Brightness of B/L :	□ Pass	□ NG ,
6. B/L Solder Method :	□ Pass	□ NG ,
7. Others :	□ Pass	□ NG ,
	>> Go to p	age 2 <<

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Winsta	ar Module Number : _			Page: 2
5 <u> </u>	Electronic Characteristics	of Module:		
1.	Input Voltage:	Pass	□ NG ,	
2.	Supply Current :	□ Pass	□ NG ,	
3.	Driving Voltage for LCD :	Pass	□NG,	
4.	Contrast for LCD :	□ Pass	□NG,	
5.	B/L Driving Method :	□ Pass	□NG,	
6.	Negative Voltage Output :	□ Pass	□NG,	
7.	Interface Function :	□ Pass	□NG,	
8.	LCD Uniformity :	□ Pass	□NG,	
9.	ESD test :	□ Pass	□ NG ,	
10.	Others :	□ Pass	□NG,	
•	•			

6 · <u>Summary</u> :

Sales signature :			
Customer Signature :	Date :	1	

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All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts.

Please contact us if you have any questions about the contents of the datasheet.

This may not be the latest version of the datasheet. Please check with us if a later version is available.





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