21.5” Full HD

High brightness color TFT-LCD module

Model: CH215CLKL-HB2

Date: May. 15th, 2012

Note: This specification is subject to change without notice

Customer： _____ **Date：** _____

Approved	**Prepared**
Date:	**Date:**

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RECORD OF REVISION

Version and Date	Page	Old description	New description	Remark
0.1 2012/5/15	All	First Edition for customer		

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1. HANDLING PRECAUTIONS

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

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2. General Description

2.1, Overview

This specification applies to the 21.5 inch color TFT-LCD module with 2-ch LVDS interface. This module supports the WUXGA -1920(H) x 1080(V) screen format and 16.7M colors (RGB 6-bits+Hi-FRC data).

2.2 Features

- Sunlight readable display, 1100nits.
- LED backlight
- WUXGA (1920x1080 pixels) full HD resolution
- RoHS Compliance

2.3 Application

Industrial Application; especial for outdoor kiosk and digital signage display.

2.4 Display Specifications

Items	Unit	Specification
Screen Diagonal	mm	546.86 (21.53”)
Active Area	mm	476.64(H) x 268.11(V)
Pixels H x V	pixels	1920(x3) x 1080
Pixels Pitch	um	248.25(per one triad) x 248.25
Pixel Arrangement		RGB Vertical stripe
Display mode		TN mode, normally white
White luminance (center)	Cd/m^2	1100 (Typ.)
Contrast ratio		1,000 (Typ.)
Optical Response Time	msec	5 ms (Typ. on/off)
Normal Input Voltage VDD	Volt	5
Power Consumption (VDD Line + LED lines)	Watt	31 (Typ.) (all black pattern)
Weight	Grams	2188(Typ.)
Physical size	mm	495.6 x 292.2 x10.3 (Typ.)
Electrical Interface		Dual Chanel LVDS
Support Colors		16.7 M colors (RGB 6-bits + Hi_FRC)
Surface Treatment		Anti-Glare, 3H
Temperature range Operating Storage (Shipping)	 ^0C ^0C	 -10 ~ 50 -20 ~ 60
RoHS Compliance		RoHS Compliance

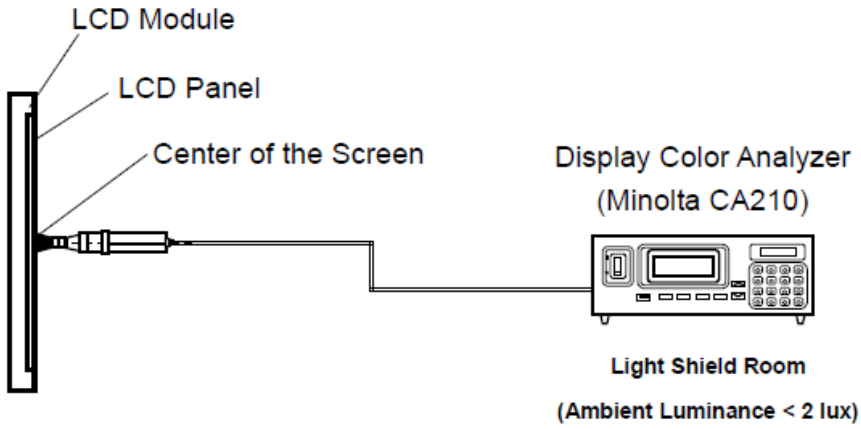
2.5 Optical Characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

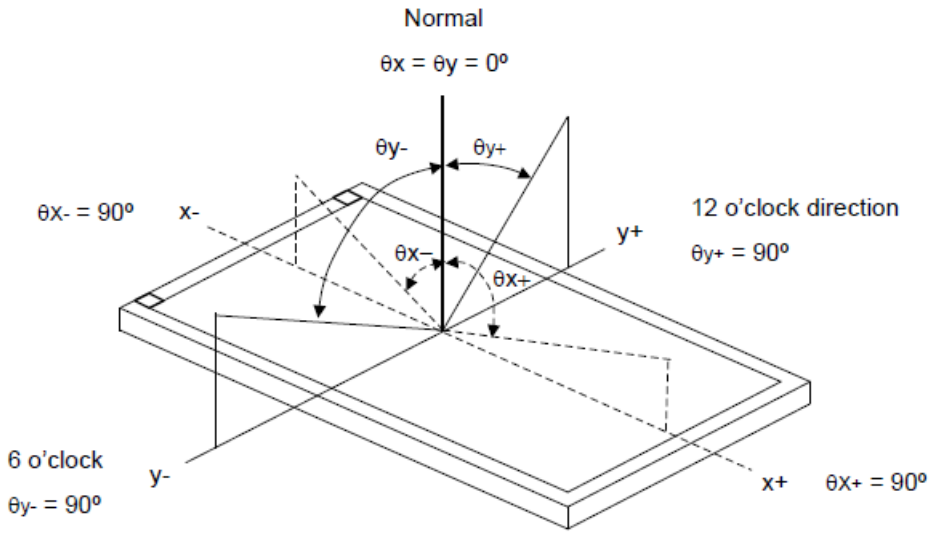
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right) CR=10 (Left)	150	170		2
		Vertical (Up) CR=10 (Down)	140	160		
Contrast Ratio		Normal Direction		1000		3
Response Time	msec	Raising time (T_{rR})		3.8	5.5	4
		Falling time (T_{rF})		1.2	2.5	
		Raising + Falling		5	8	
Color / Chromaticity Coordinates (CIE)		Red x	Typ -0.03	0.64	Typ +0.03	5
		Red y		0.33		
		Green x		0.33		
		Green y		0.63		
		Blue x		0.15		
		Blue y		0.05		
Color coordinates (CIE) White		White x		0.320		
		White y		0.350		
Center Luminance	Cd/m^2		880	1100		6
Luminance Uniformity	%		60	70		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



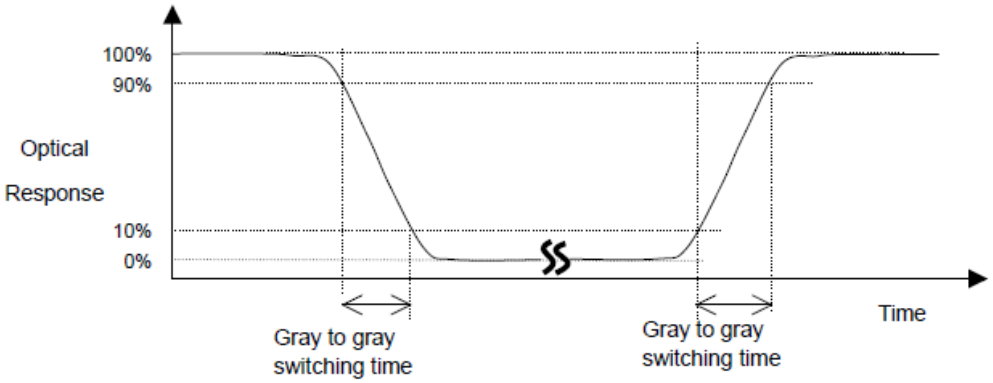
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minta BM-7

Note 4: Definition of Response time

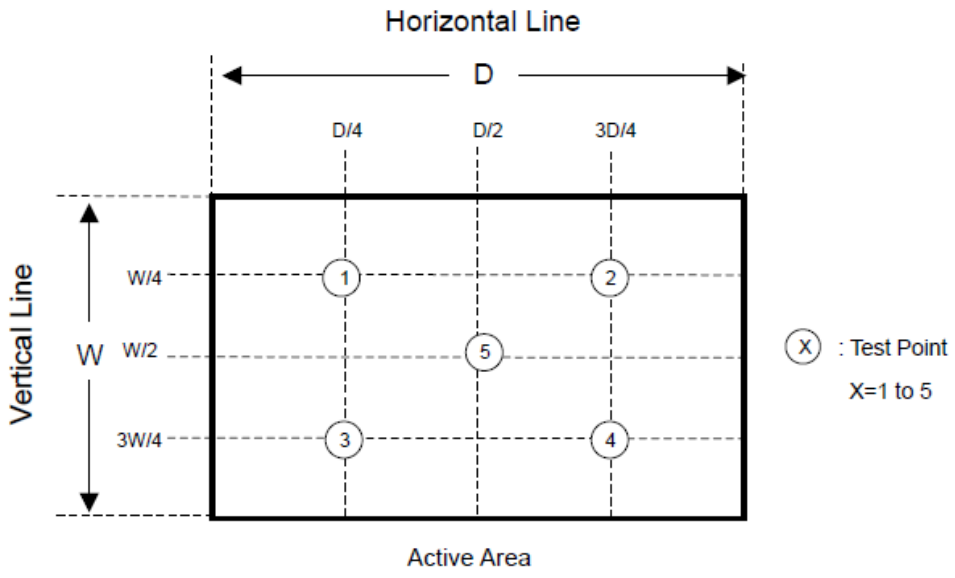
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minta BM-7

Note 6: Center luminance is measured by Minta BM-7

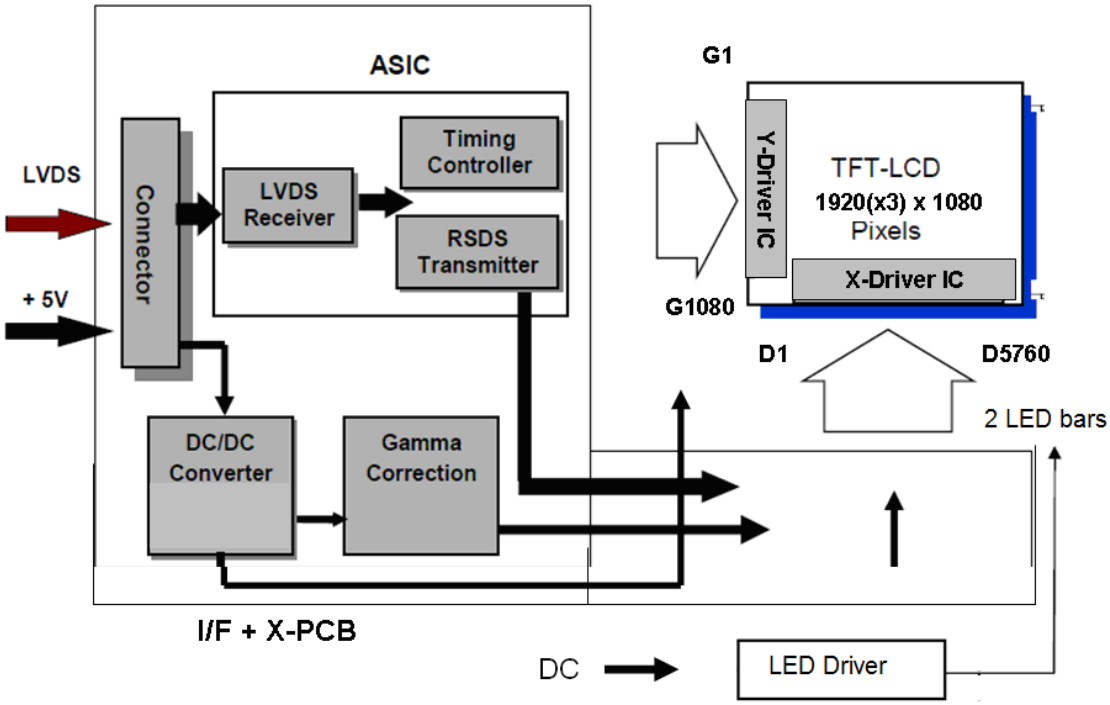
Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minta BM-7



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. **Functional Block Diagram**

The following diagram shows the functional block of the 21.5 inches Color TFT-LCD Module:



I/F PCB Interface:

FI-XPB30SRLA-HF11-R3000 (JAE)

or 187121-30091 (P-TWO)

Mating Type:

FI-X30HL (Locked Type)

4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD Module

Items	Symbol	Min	Max	Unit	Conditions
Logic/ LCD drive voltage	VDD	0	6.0	Volt	Note 1, 2

4.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED Current	I LED		540	mA	Note 1, 2

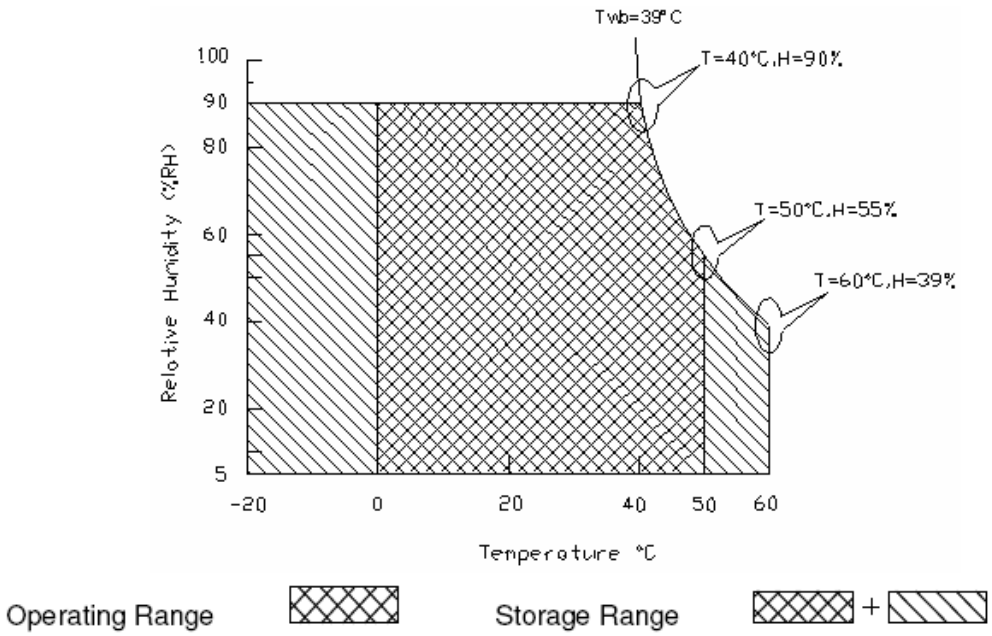
4.3 Absolute Ratings of Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-10	-	50	^{0}C	Note 3
Operation Humidity	H_{OP}	5		90	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).



5. Electrical characteristics

5.1 TFT LCD Module

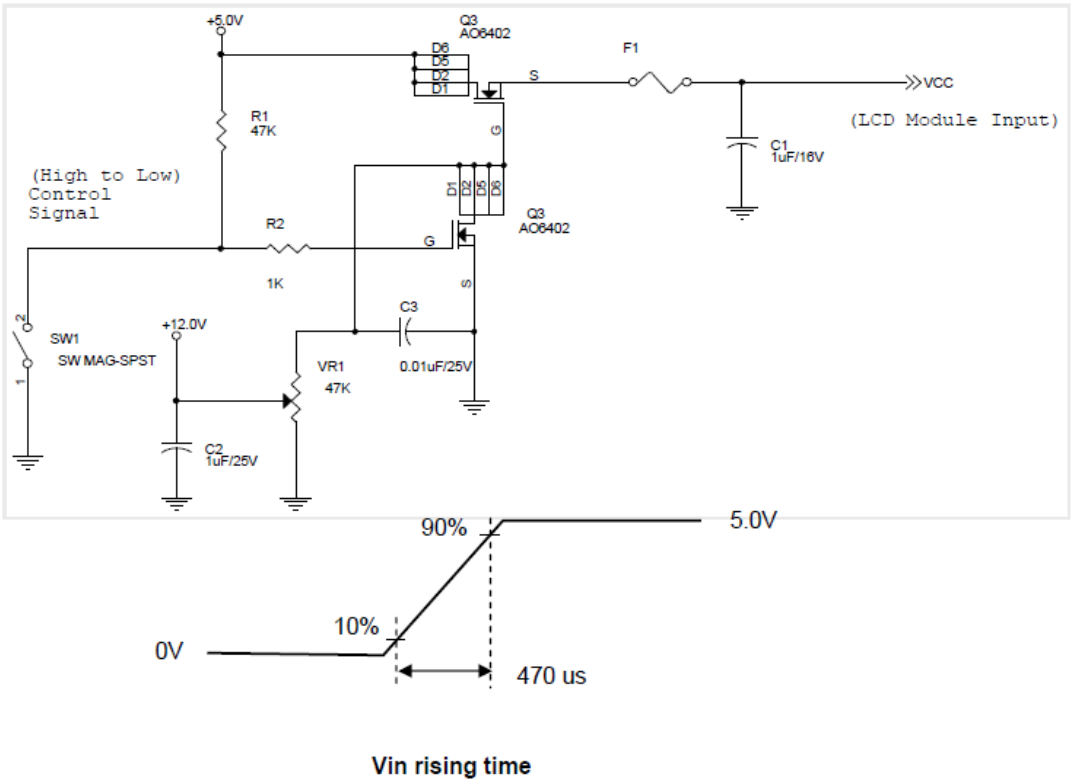
5.1.1 Power Specification

Input power specifications are as follows

Symbol	Parameter	Min	Typ.	Max	Unit	Conditions
VDD	Logic/ LCD Drive Voltage	4.5	5	5.5	Volt	+/- 10%
IDD	Input current		0.92	1.1	A	VDD=5V, All black pattern. At 75Hz, +30%
PDD	VDD power		4.6	5.5	W	VDD=5V, All black pattern. At 75Hz,
IRush	Inrush current			2	A	Note 1
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			500	mV p-p	VDD=5V, All black pattern. At 75Hz,

Note 1: Measurement conditions:

The duration of rising time of input power is 470 us.



Vin rising time

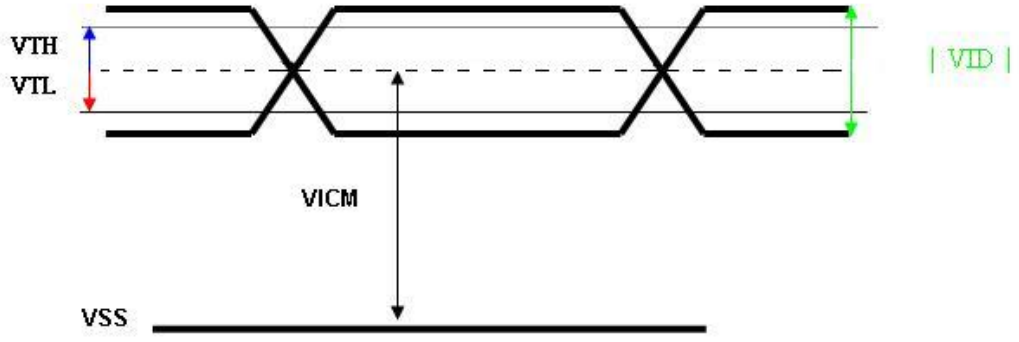
5.1.2 Signal Electrical Characteristics

Input signal shall be low or Hi-Z state when VDD is off. Please refer to specification of SN75LVDS82DGG (Texas Instruments) in detail.

Characteristics of each signal are as following:

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VTH	Differential Input High Threshold		+50	+100	mV	VICM = 1.2V NOTE 1
VTL	Differential Input Low Threshold	-100	-50		mV	VICM = 1.2V NOTE 1
|VID|	Input Differential Voltage	100		600	mV	NOTE 1
VICM	Differential Input Common Mode Voltage	+1.0	+1.2	+1.5	V	VTH-VTL = 200mV(MAX) NOTE 1

Note 1: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline is under stable conditions at 25℃ (Room Temperature):

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		28.8		[V]	
LED current (IL)		480		[mA]	,
LED Life Time(LTLED)		40000		[Hour]	1

Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and typical LED Current at 420 mA .

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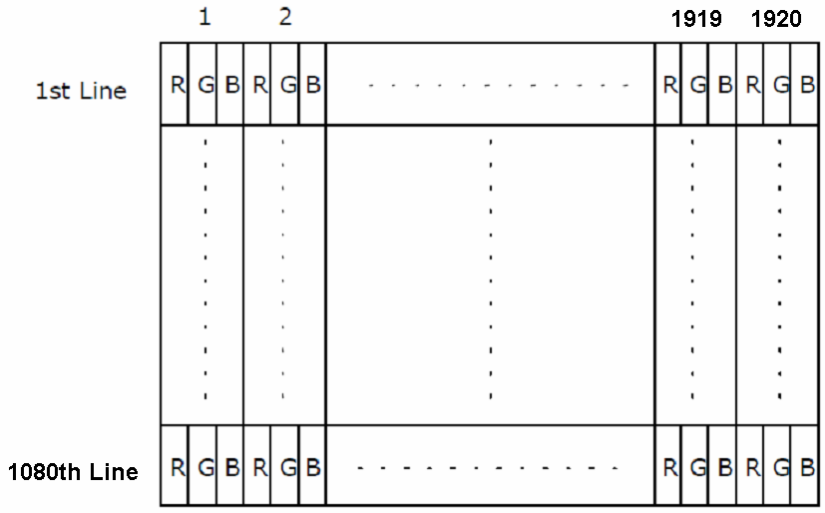
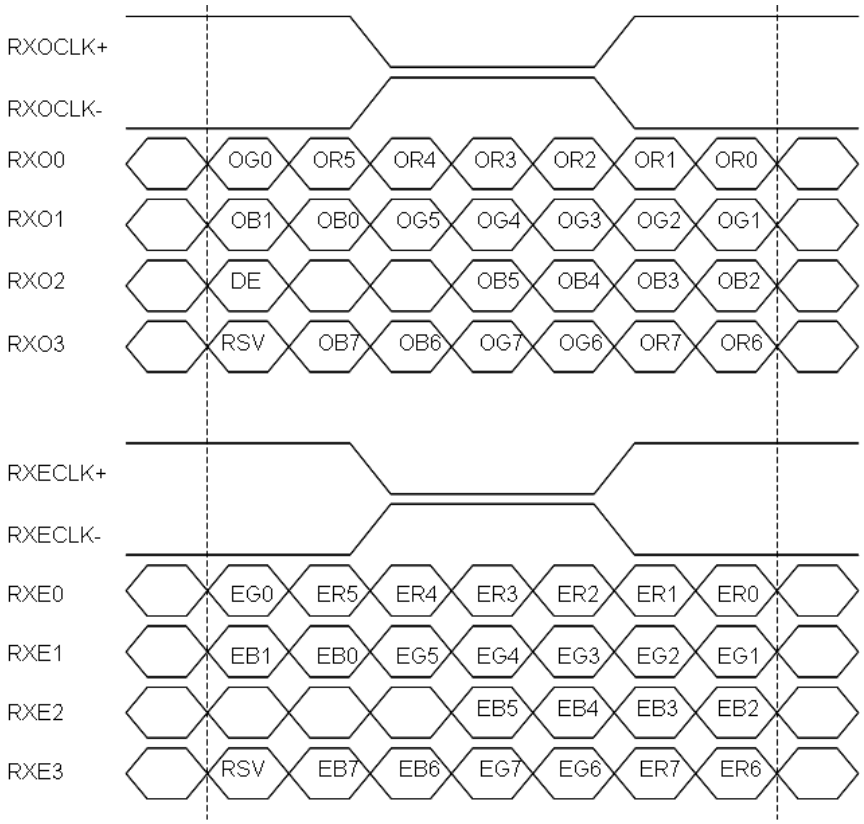
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Note 1: R/G/B data 7:MSB, R/G/B data 0:LSB "O"="First Pixel Data"

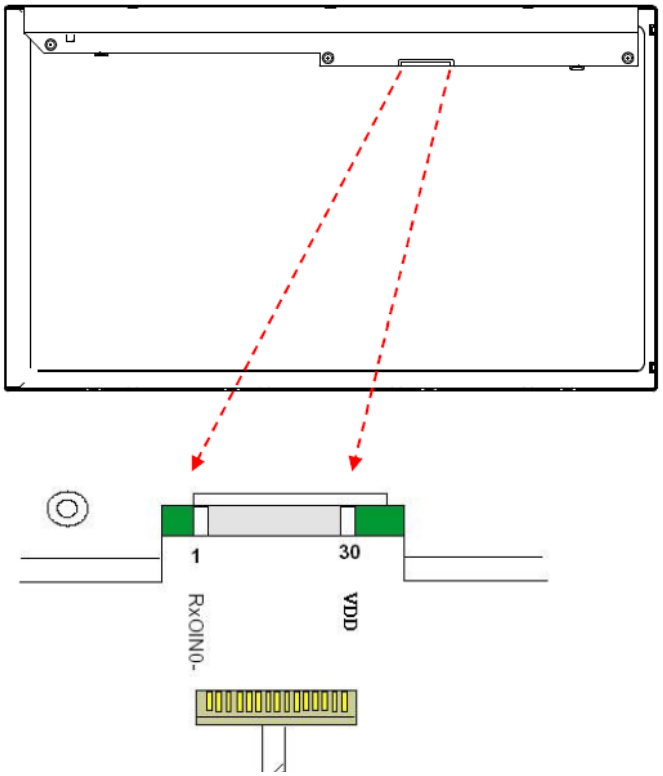
"E"="Second Pixel Data"

6.3 Signal Description

The module using one LVDS receiver SN75LVDS82(Texas Instruments). LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling). The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

PIN#	Signal Name	DESCRIPTION
1	RxOIN0-	Negative LVDS differential data input (Odd data)
2	RxOIN0+	Positive LVDS differential data input (Odd data)
3	RxOIN1-	Negative LVDS differential data input (Odd data)
4	RxOIN1+	Positive LVDS differential data input (Odd data)
5	RxOIN2-	Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
6	RxOIN2+	Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
7	GND	Power Ground
8	RxOCLK-	Negative LVDS differential clock input (Odd clock)
9	RxOCLK+	Positive LVDS differential clock input (Odd clock)
10	RxOIN3-	Negative LVDS differential data input (Odd data)
11	RxOIN3+	Positive LVDS differential data input (Odd data)
12	RxEIN0-	Negative LVDS differential data input (Even data)
13	RxEIN0+	Positive LVDS differential data input (Even data)
14	GND	Power Ground
15	RxEIN1-	Negative LVDS differential data input (Even data)
16	RxEIN1+	Positive LVDS differential data input (Even data)
17	GND	Power Ground
18	RxEIN2-	Negative LVDS differential data input (Even data)
19	RxEIN2+	Positive LVDS differential data input (Even data)
20	RxECLK-	Negative LVDS differential clock input (Even clock)
21	RxECLK+	Positive LVDS differential clock input (Even clock)
22	RxEIN3-	Negative LVDS differential data input (Even data)
23	RxEIN3+	Positive LVDS differential data input (Even data)
24	GND	Power Ground
25	NC	Do not connect (for test only)
26	NC	Do not connect (for test only)
27	NC	Do not connect (for test only)
28	VDD	Power +5V
29	VDD	Power +5V
30	VDD	Power +5V

Note 1: Start from left side



Note2: Input signals of odd and even clock shall be the same timing.

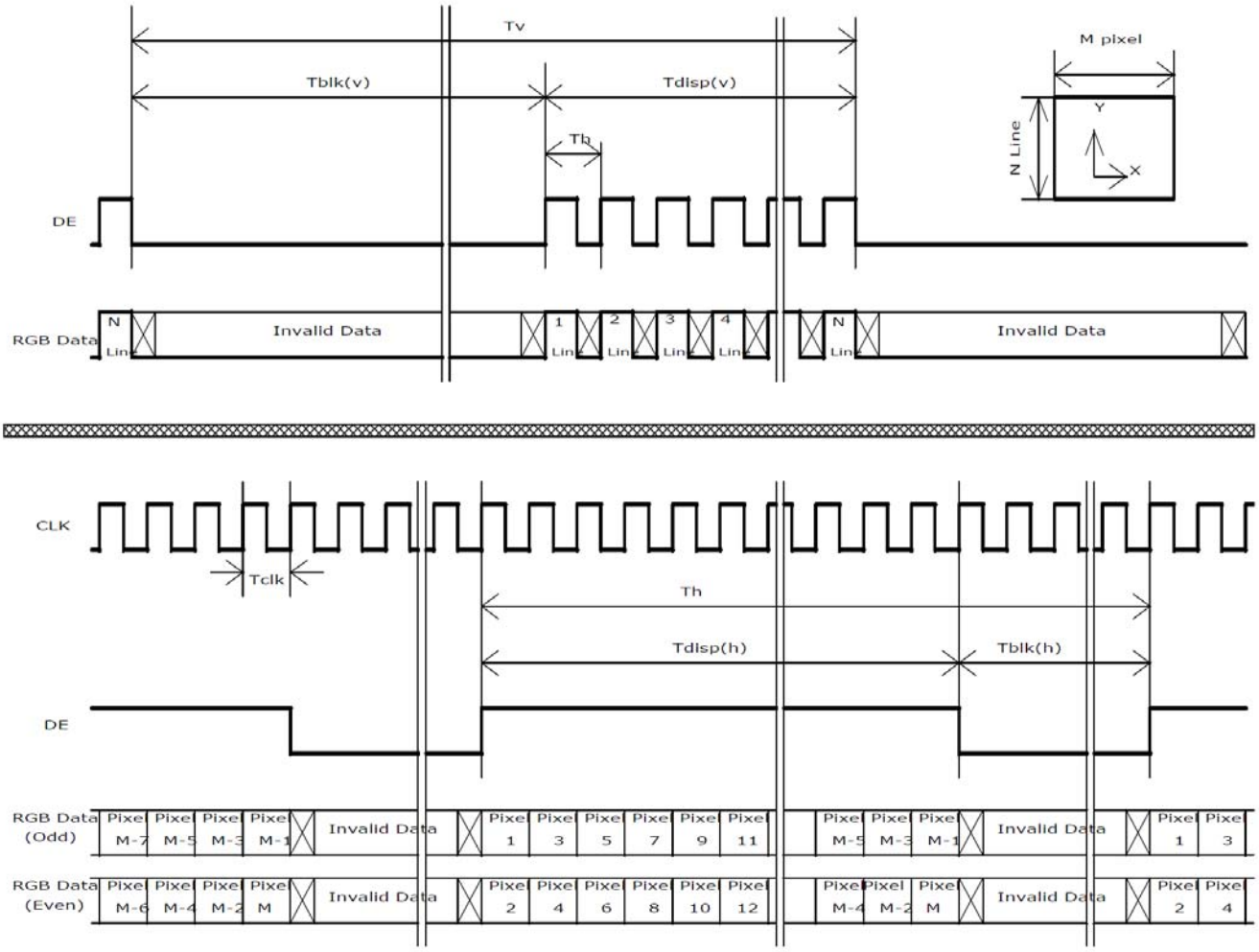
6.4. Timing Characteristics

Basically, interface timing described here is not actual input timing of LCD module but close to output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

Items		Symbol	Min.	Typ.	Max.	Unit
H-section	Period	Th	1034	1060	2047	Tclk
	Display Area	Tdisp(h)	960	960	960	Tclk
	Blanking	Tblk(h)	74	100	1087	Tclk
V-section	Period	Tv	1088	1120	2047	Th
	Display Area	Tdisp(h)	1080	1080	1080	Th
	Blanking	Tblk(h)	8	40	967	Th
Clock	Period	Tclk	25	13.3	11.1	nS
	Frequency	Freq	40	75	90	MHz
Frame Rate		F	50	60	75	Hz

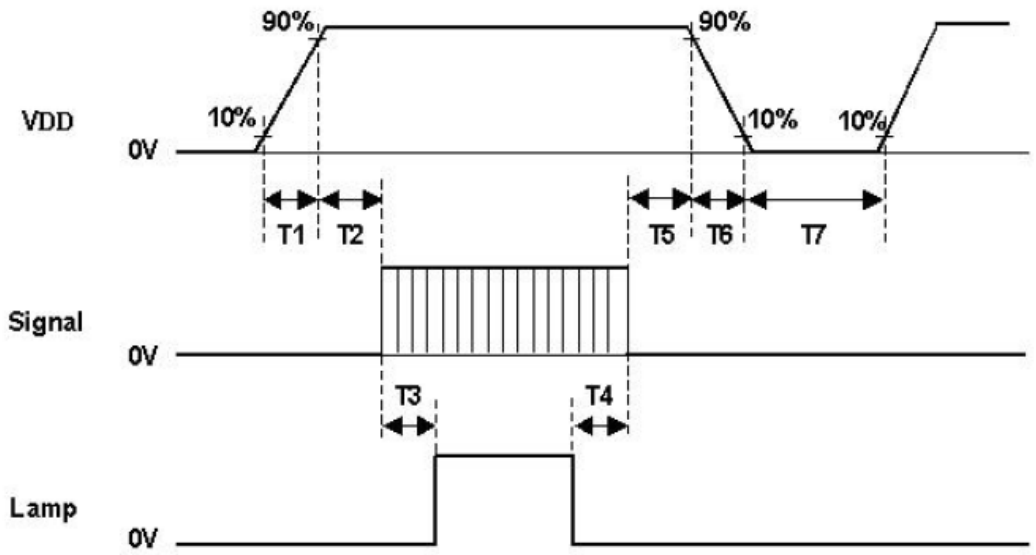
Note: DE mode only

6.5 Timing Diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	[msec]
T2	0	-	50	[msec]
T3	200	-	-	[msec]
T4	200	-	-	[msec]
T5	0	16	50	[msec]
T6	-	-	100	[msec]
T7	1000	-	-	[msec]

7.0 Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	JAE / P-TWO
Type Part Number	FI-XPB30SRLA-HF11-R3000 (JAE) or 187121-30091 (P-TWO)
Mating Housing Part Number	FI-X30HL(Locked type)

7.1.1 Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	GND	8	RxOCLK-
9	RxOCLK+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	GND
15	RxEIN1-	16	RxEIN1+
17	GND	18	RxEIN2-
19	RxEIN2+	20	RxECLK-
21	RxECLK+	22	RxEIN3-
23	RxEIN3+	24	GND
25	NC	26	NC
27	NC	28	VDD
29	VDD	30	VDD

7.2 Backlight Unit

Pin No.	Symbol	I/O	Function	Remark
1	VLED+	P	Power for LED backlight anode	White
2	VLED-	P	Power for LED backlight cathode	Black

LED Light Bar Connector is used for the integral backlight system. The recommended model is BHSR-02VS-1 manufactured by JST.

8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	3
Low Temperature Operation (LTO)	Ta= -10℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

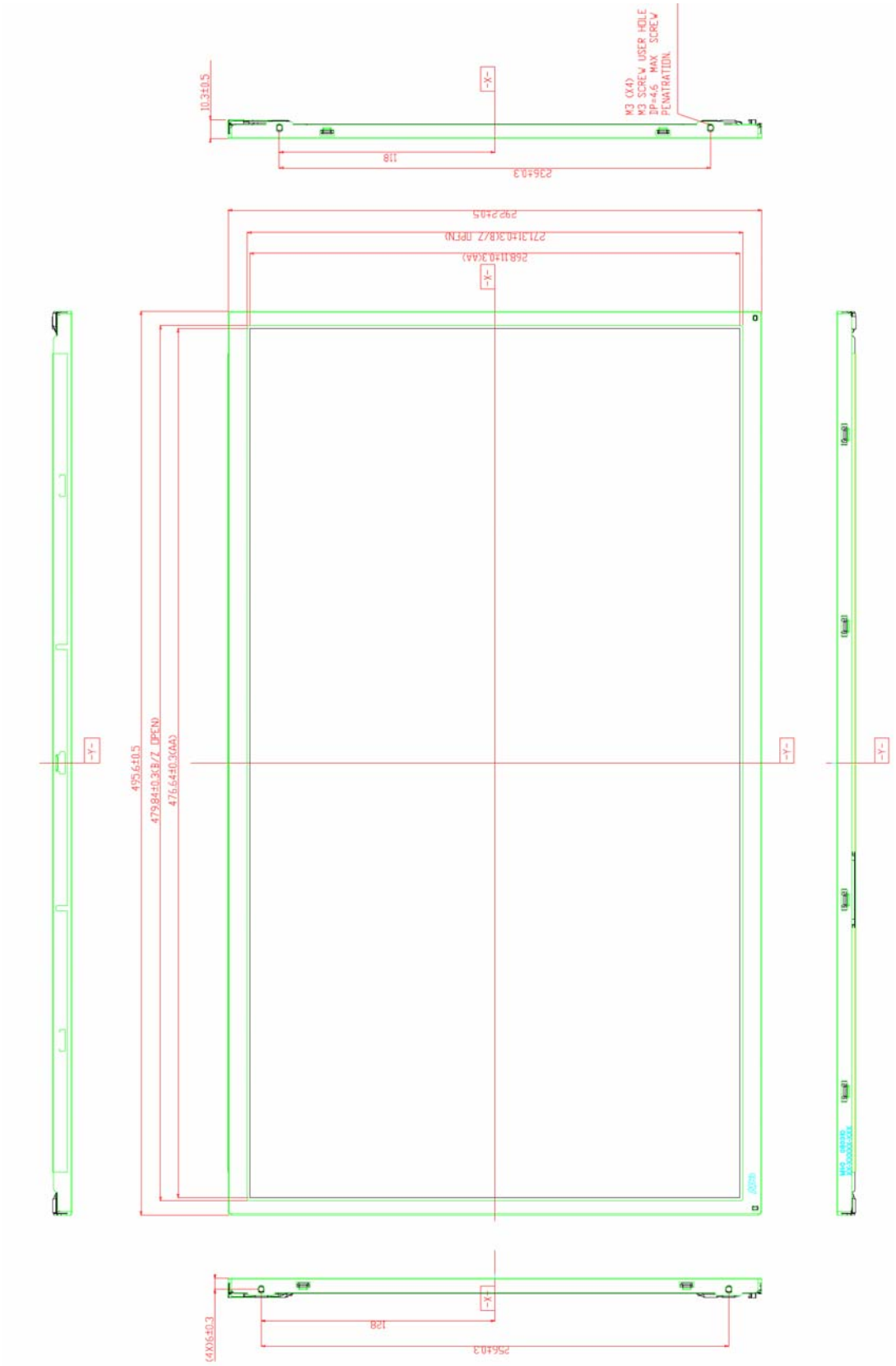
Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: The test items are tested by open frame type chassis.

9. Shipping Label & Package

(TBD)

10. Mechanical Characteristic



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