

Product Specification

Chefree Technology Corp.



19.0" SXGA High brightness color TFT-LCD module

Model: CH190CLJL-HB1

Date: May 09th, 2011

Note: This specification is subject to change without notice

Customer :	
	Date :
Approved	Prepared
Data	Data

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RECORD OF REVISION

Vers	ion and Date	Page	Old description	New description	Remark
Vers 0.1	ion and Date 2011/05/09	Page	Old description First Edition for customer	New description	Remark

1. HANDLING PRECAUTIONS

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of TFTLCD panel.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11)After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 13)Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.

2. General Description

2.1, Overview

This is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display, a driver circuit, and a backlight system. The display supports the SXGA+ (1280(H) x 1024(V)) screen format and 16.7M colors (RGB 6-bits+Hi-RFC data). All input signals are 2 Channel LVDS interface compatible.

2.2 Features

- 1000nits high brightness
- LED backlight
- Wide operation temperature
- RoHS Compliance

2.3 Application

Industrial Application.

2.4 Display Specifications

Items	Unit	Specification
Screen Diagonal	inch	19.0"
Active Area	mm	376.32(H) × 301.06(V)
Pixels H x V	pixels	1280 × 3(RGB) × 1024
Pixels Pitch	um	0.294(per one triad) × 0.294
Pixel Arrangement		RGB Vertical stripe
Display mode		TN mode, normally white
White luminance (center)	Cd/m ²	1000 (Typ.)
Contrast ratio		1000 (Typ.)
Optical Response Time	msec	5 ms (Typ. on/off)
Normal Input Voltage VDD	Volt	5.0
Power Consumption	Watt	32 (Typ.)
(VDD Line + LED L Line)		
Weight	Grams	2500 (Typ.)
Physical size	mm	396 (H) x 324 (V) x 18.5 (D) (Typ)
Electrical Interface		2 Chanel LVDS
Support Colors		16.7M colors (RGB 6-bits +Hi-FRC data)
Surface Treatment		Anti-Glare, 3H
Temperature range		
Operating	°C	-20 ~ 60 (LCD surface temperature)
Storage (Shipping)	°C	-20 ~ 70
RoHS Compliance		RoHS Compliance

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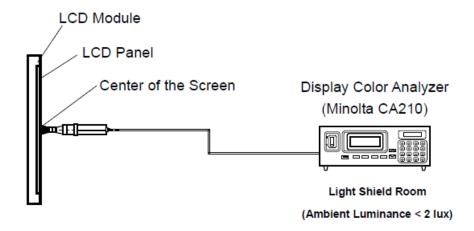
2.5 Optical Characteristics

The following optical characteristics are measured under stable condition at 25 $^{\circ}\text{C}$

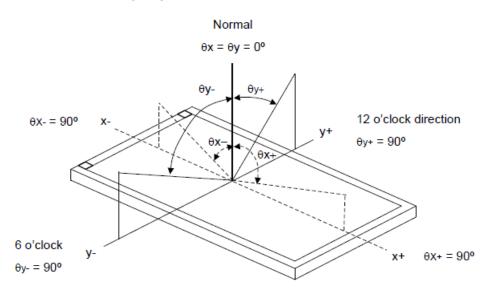
Items	Unit	Conditions	Min.	Тур.	Max.	Note
Minusiana anala	Dan	Horizontal (Right) CR=10 (Left)	160	170		
Viewing angle	Deg.	Vertical (Up) CR=10 (Down)	150	160		2
Contrast Ratio		Normal Direction	800	1000		3
		Raising time (T _{rR})		3.6		
Response Time	msec	Falling time (T _{rF})		1.4		4
		Raising + Falling		5		
		Red x	-0.03		+0.03	
		Red y				
Color / Chromaticity		Green x				
Coordinates (CIE)		Green y				5
		Blue x				5
		Blue y				
Color coordinates		White x		0.313		
(CIE) White		White y		0.329		
Center Luminance	Cd/m ²		850	1000		6
Luminance Uniformity	%			70		7
Crosstalk (in 60 Hz)	%				1	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



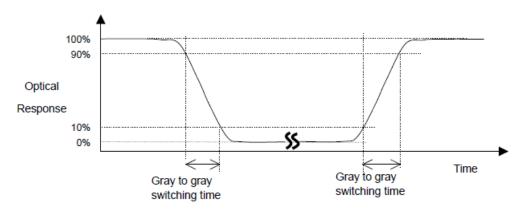
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Topcon BM-7

Note 4: Definition of Response time

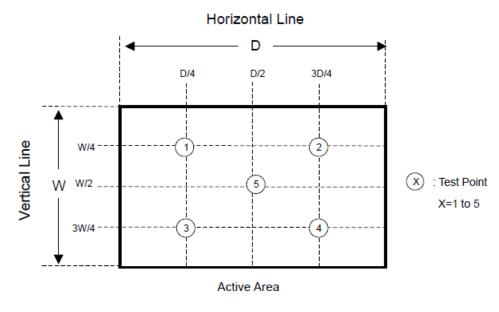
The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Topcon BM-7

Note 6: Center luminance is measured by Topcon BM-7

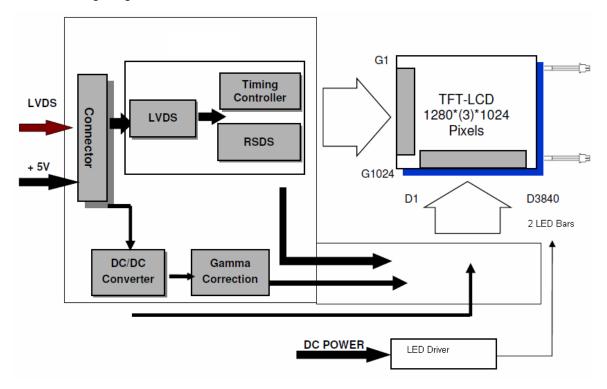
Note 7: Luminance uniformity of these 5 points is defined as below and measured by Topcon BM-7



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Functional Block Diagram

The following diagram shows the functional block of the 19 inches Color TFT-LCD Module:



I/F PCB Interface:

FI-XB30SSL-HF15 / MSBKT2407P30HB

Mating Type:

FI-X30HL (Locked Type)

FI-X30H (Unlocked Type)

4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD Module

Items	Symbol	Min	Max	Unit	Conditions
Logic/ LCD drive	Vin	-0.3	6	Volt	Note 1, 2
voltage					

4.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED Current	I LED		640	mA	Note 1, 2

4.3 Absolute Ratings of Environment

Items	Symbol	Values			Unit	Conditions		
	Symbol	Min.	Тур.	Max.	Offic	Conditions		
Operation temperature	T _{OP}	-20	-	60	°C			
Operation Humidity	H _{OP}	8		90	%	Note 2		
Storage temperature	T _{ST}	-20		60	°C	Note 3		
Storage Humidity	H _{ST}	8		90	%			

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

5. Electrical characteristics

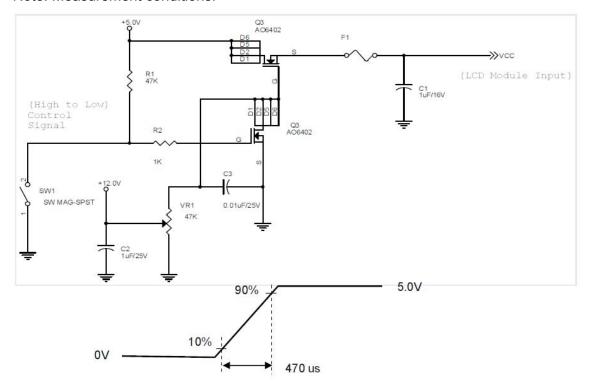
5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows

Symbol	Parameter	Min	Тур	Max	Unit	Condition
VDD	Logic/LCD Drive Voltage	4.50	5.00	5.50	[Volt]	±10%
IDD	Input Current	-	1.10	1.31	[A]	VDD= 5.0V,All black Pattern, At 60Hz
IDD	Input Current	-	1.37	1.63	[A]	VDD= 5.0V,H-Stripe Pattern, At 75Hz Note1
PDD	VDD Power	-	5.50	6.55	[Watt]	VDD= 5.0V,All black Pattern, At 60Hz
PDD	VDD Power	-	6.85	8.15	[Watt]	VDD= 5.0V,H-Stripe Pattern, At 75Hz
IRush	Inrush Current	-	-	2.5	[A]	Note2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	VDD= 5.0V,All black Pattern, At 75Hz

Note: Measurement conditions:



Vin rising time

5.2 Backlight Unit

Parameter guideline is under stable conditions at 25°C (Room Temperature):

Parameter	Min	Тур	Max	Unit	Note
LED voltage (VL)		27		[V]	2
LED current (IL)		480		[mA]	2,
LED Life Time(LTLED)		50,000		[Hour]	1

- Note 1: The "LED life time" is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25° C and typical LED Current at 480 mA .
- Note 2: The LED driving condition is defined for each LED module.
- Note 3: The variance of LED Light Bar power consumption is $\pm 10\%$. Calculator value for reference (IL × VL × 2 = PLED)
- Note 4: LED Light Bar Connector is used for the integral backlight system. The recommended model is BHSR-02VS-1 manufactured by JST

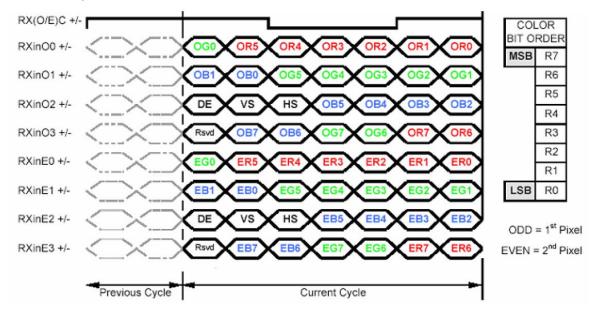
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	0			1			1	27	9	12	280	0
1st Line	R G	В	R	G	В		R	G	В	R	G	В
				!		1						
	1			ı		ı		ı				
				•		•		•			•	
				:		:		÷			÷	
				•		•		•			•	
								1				
				<u>'</u>		1					<u>'</u>	
1024th Line	R G	В	R	G	В		R	G	В	R	G	В

6.2 The Input Data Format



Note1: Normally DE mode only. VS and HS on EVEN channel are not used.

Note2: Please follow VESA.

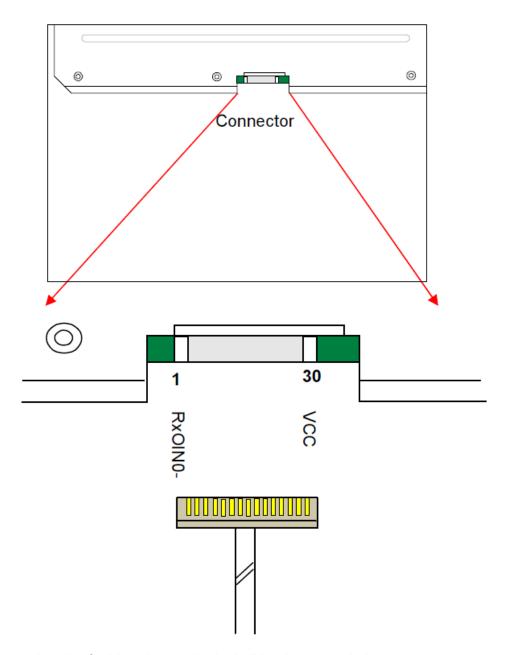
Note3: 8-bit in

6.3 Signal Description

The module using a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

1 RxOIN0- Negative LVDS differential data input (Odd data) 2 RxOIN1- Positive LVDS differential data input (Odd data) 3 RxOIN1- Negative LVDS differential data input (Odd data) 4 RxOIN1+ Positive LVDS differential data input (Odd data) 5 RxOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RxOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential data input (Even data) 21 RxECLKIN- Negative LVDS differential data input (Even data) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3- Negative LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply			into even pixeis.
2 RxOIN0+ Positive LVDS differential data input (Odd data) 3 RxOIN1- Negative LVDS differential data input (Odd data) 4 RxOIN2- Negative LVDS differential data input (Odd data) 5 RxOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RxOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RxOCLKIN+ Positive LVDS differential clock input (Odd data) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Even data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0- Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) <td>PIN#</td> <td>SIGNAL NAME</td> <td>DESCRIPTION</td>	PIN#	SIGNAL NAME	DESCRIPTION
RXOIN1- Negative LVDS differential data input (Odd data) RXOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXOIN3- Negative LVDS differential clock input (Odd clock) RXOIN3- Negative LVDS differential clock input (Odd data) RXOIN3- Negative LVDS differential data input (Odd data) RXOIN3- Negative LVDS differential data input (Odd data) RXIN0- Negative LVDS differential data input (Odd data) RXEIN0- Negative LVDS differential data input (Even data) RXEIN0- Negative LVDS differential data input (Even data) RXEIN1- Negative LVDS differential data input (Even data) RXEIN2- Negative LVDS differential data input (Even data) RXEIN2- Negative LVDS differential data input (Even data) RXELN2- Negative LVDS differential data input (Even data) RXECLKIN- Negative LVDS differential clock input (Even clock) RXECLKIN- Negative LVDS differential data input (Even data) RXECLKIN- Negative LVDS differential data input (Even data)	1	RxOIN0-	Negative LVDS differential data input (Odd data)
4 RXOIN1+ Positive LVDS differential data input (Odd data) 5 RXOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RXOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RXOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RXOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Negative LVDS differential data input (Even data) 16 RXEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXECLKIN+ Positive LVDS differential clock input (Even clock) 22 RXEIN3- Negative LVDS differential clock input (Even data) 23 RXEIN3- Positive LVDS differential clock input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	2	RxOIN0+	Positive LVDS differential data input (Odd data)
5 RxOIN2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RxOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3- Negative LVDS differential data input (Even data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0- Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2- Negative LVDS differential clock input (Even data) 20 RxECLKIN+ Positive LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential data input (Even data) 2	3	RxOIN1-	Negative LVDS differential data input (Odd data)
6 RxOIN2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 VSS Power Ground 8 RxOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RxOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even data) 21 RxECLKIN- Positive LVDS differential clock input (Even data) 22 RxEIN3- Negative LVDS differential clock input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	4	RxOIN1+	Positive LVDS differential data input (Odd data)
7 VSS Power Ground 8 RXOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RXOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Negative LVDS differential data input (Even data) 16 RXEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXECLKIN- Positive LVDS differential clock input (Even clock) 22 RXEIN3- Negative LVDS differential clock input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	5	RxOIN2-	Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
8 RXOCLKIN- Negative LVDS differential clock input (Odd clock) 9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RXOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Negative LVDS differential data input (Even data) 16 RXEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXECLKIN+ Positive LVDS differential clock input (Even clock) 22 RXEIN3- Negative LVDS differential clock input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	6	RxOIN2+	Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
9 RXOCLKIN+ Positive LVDS differential clock input (Odd clock) 10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RXOIN3+ Positive LVDS differential data input (Odd data) 12 RXEIN0- Negative LVDS differential data input (Even data) 13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Negative LVDS differential data input (Even data) 16 RXEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXECLKIN+ Positive LVDS differential clock input (Even data) 22 RXEIN3- Negative LVDS differential data input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	7	VSS	Power Ground
10 RxOIN3- Negative LVDS differential data input (Odd data) 11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	8	RxOCLKIN-	Negative LVDS differential clock input (Odd clock)
11 RxOIN3+ Positive LVDS differential data input (Odd data) 12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even data) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	9	RxOCLKIN+	Positive LVDS differential clock input (Odd clock)
12 RxEIN0- Negative LVDS differential data input (Even data) 13 RxEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	10	RxOIN3-	Negative LVDS differential data input (Odd data)
13 RXEIN0+ Positive LVDS differential data input (Even data) 14 VSS Power Ground 15 RXEIN1- Negative LVDS differential data input (Even data) 16 RXEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RXEIN2- Negative LVDS differential data input (Even data) 19 RXEIN2+ Positive LVDS differential data input (Even data) 20 RXECLKIN- Negative LVDS differential clock input (Even clock) 21 RXECLKIN+ Positive LVDS differential clock input (Even data) 22 RXEIN3- Negative LVDS differential data input (Even data) 23 RXEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	11	RxOIN3+	Positive LVDS differential data input (Odd data)
14 VSS Power Ground 15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	12	RxEIN0-	Negative LVDS differential data input (Even data)
15 RxEIN1- Negative LVDS differential data input (Even data) 16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply	13	RxEIN0+	Positive LVDS differential data input (Even data)
16 RxEIN1+ Positive LVDS differential data input (Even data) 17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	14	VSS	Power Ground
17 VSS Power Ground 18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	15	RxEIN1-	Negative LVDS differential data input (Even data)
18 RxEIN2- Negative LVDS differential data input (Even data) 19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	16	RxEIN1+	Positive LVDS differential data input (Even data)
19 RxEIN2+ Positive LVDS differential data input (Even data) 20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	17	VSS	Power Ground
20 RxECLKIN- Negative LVDS differential clock input (Even clock) 21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	18	RxEIN2-	Negative LVDS differential data input (Even data)
21 RxECLKIN+ Positive LVDS differential clock input (Even clock) 22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	19	RxEIN2+	Positive LVDS differential data input (Even data)
22 RxEIN3- Negative LVDS differential data input (Even data) 23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	20	RxECLKIN-	Negative LVDS differential clock input (Even clock)
23 RxEIN3+ Positive LVDS differential data input (Even data) 24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	21	RxECLKIN+	Positive LVDS differential clock input (Even clock)
24 VSS Power Ground 25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	22	RxEIN3-	Negative LVDS differential data input (Even data)
25 VSS Power Ground 26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	23	RxEIN3+	Positive LVDS differential data input (Even data)
26 NC Do not connect (for AUO test) 27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	24	VSS	Power Ground
27 VSS Power Ground 28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	25	VSS	Power Ground
28 VCC +5.0V Power Supply 29 VCC +5.0V Power Supply	26	NC	Do not connect (for AUO test)
29 VCC +5.0V Power Supply	27	VSS	Power Ground
	28	VCC	+5.0V Power Supply
30 VCC +5.0V Power Supply	29	VCC	+5.0V Power Supply
30 VOO 13.0V FOWEI Supply	30	VCC	+5.0V Power Supply

Note1: Start from left side



Note2: Input signals of odd and even clock shall be the same timing.

Note3: Please follow VESA.

6.4 Timing Characteristics

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

6.4.1 Timing Characteristics

Signal	Item	Symbol	Min	Тур	Max	Unit
	Period	Tv	1032	1066	1150	Th
Vertical	Active	Tdisp(v)	1024	1024	1024	Th
Section	Blanking	Tbp(v)+Tfp(v)+PWvs	8	42	126	Th
	Period	Th	780	844	2047	Tclk
Horizontal	Active	Tdisp(h)	640	640	640	Tclk
Section	Blanking	Tbp(h)+Tfp(h)+PWhs	140	204	-	Tclk
Olask	Period	Tdk	22.2	18.52	14.81	ns
Clock	Frequency	Freq.	45	54	67.5	MHz

50

60

75

Hz

1/Tv

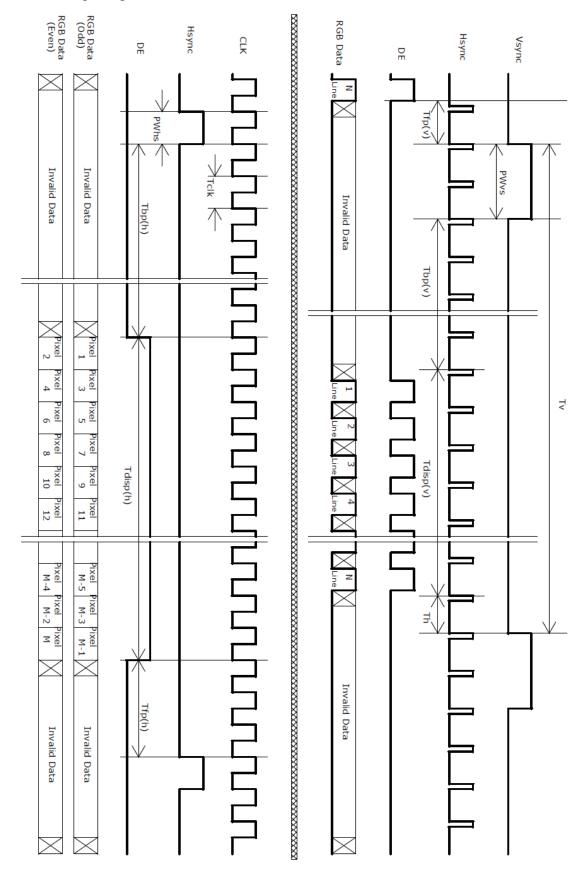
Note:

Frame Rate

DE Only mode operation.

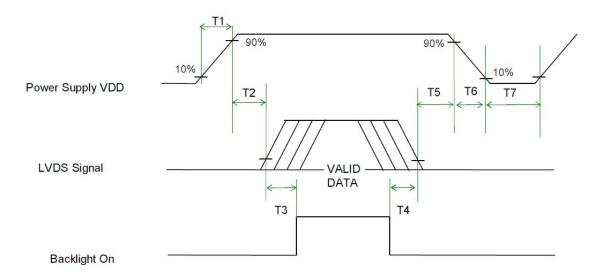
Frequency

6.4.2 Timing Diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as below. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power ON/OFF sequence timing

Parameter		Value	Unit	
Parameter	Min.	Тур.	Max.	Offic
T1	0.5	-	10	[ms]
T2	0	40	50	[ms]
Т3	300	-	-	[ms]
T4	300	-	-	[ms]
T5	0.5	16	50	[ms]
T6	-	-	-	[ms]
Т7	1000	-	-	[ms]

Note: The values of the table are follow PSWG.

7.0 Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	JAE / STM
Type Part Number	FI-XB30SSL-HF15 / MSBKT2407P30HB
Mating Housing Part Number	FI-X30HL

Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	VSS	8	RxOCLKIN-
9	RxOCLKIN+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	VSS
15	RxEIN1-	16	RxEIN1+
17	VSS	18	RxEIN2-
19	RxEIN2+	20	RxECLKIN-
21	RxECLKIN+	22	RxEIN3-
23	RxEIN3+	24	VSS
25	VSS	26	NC
27	VSS	28	VCC
29	VCC	30	VCC

7.2 Backlight Unit: LED Connector

Pin No.	Symbol	I/O	Function	Remark
1	VLED+	Р	Power for LED backlight anode	White
2	VLED-	Р	Power for LED backlight cathode	Black

LED Light Bar Connector is used for the integral backlight system. The recommended model is BHSR-02VS-1 manufactured by JST.

8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 60℃, 50%RH, 300hours	3
Low Temperature Operation (LTO)	Ta= -20°C, 300hours	
High Temperature Storage (HTS)	Ta= 70℃, 300hours	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV,	2
	150pF(330Ω) 1sec, 9 points, 25	
	times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω)	2
	1sec 9 points, 25 times/ point.	

- Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.
- Note 2: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.
- Note 3: The test items are tested by open frame type chassis.

9. Shipping Label & Package (TBD)

(Original panel package)

10. Mechanical Characteristic

