

CUSTOMER' S APPROVAL SPECIFICATIONS

MODEL: CH170CLJL-001

(Complied with RoHS)



ISSUE:DEC.12.2013

Spec Condition:preliminary

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| CUSTOMER | | CHEFREE | |
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| APPROVAL | <i>A Joly</i> | <i>Joly</i> | <i>lan</i> |

2.RECORD OF REVISION

| REV | DATE | PAGE | SUMMARY |
|-----|------------|------|---|
| 0.1 | 2013.12.12 | ALL | Preliminary specification was first issued. |
| | | | |

3.MECHANICAL SPECIFICATIONS

| | | |
|------|-----------------------|------------------------------------|
| (1) | Number Of Dots (Dots) | 1280(R.G.B) X 1024 |
| (2) | Module Size(mm) | 358.5(H) X 296.5(V) X 17 (D) * |
| (3) | Active Area(mm) | 337.920(H) X 270.336(V) |
| (4) | Pixel Pitch(mm) | 0.264 (H) X 0.264(V) |
| (5) | LCD / Polarizer Model | TFT , Transmissive, Normally/White |
| (6) | Backlight Color | White, LED |
| (7) | Surface Treatment | Anti-glare, Hard-Coating(3H) |
| (8) | Electrical Interface | LVDS Interface |
| (9) | Color Configuration | R.G.B. Vertical Stripe |
| (10) | Module Weight(g) | TBD |

Note 1. Viewing direction for best image quality is different from TFT definition, there is the 180 degrees shift.

Distributed by:

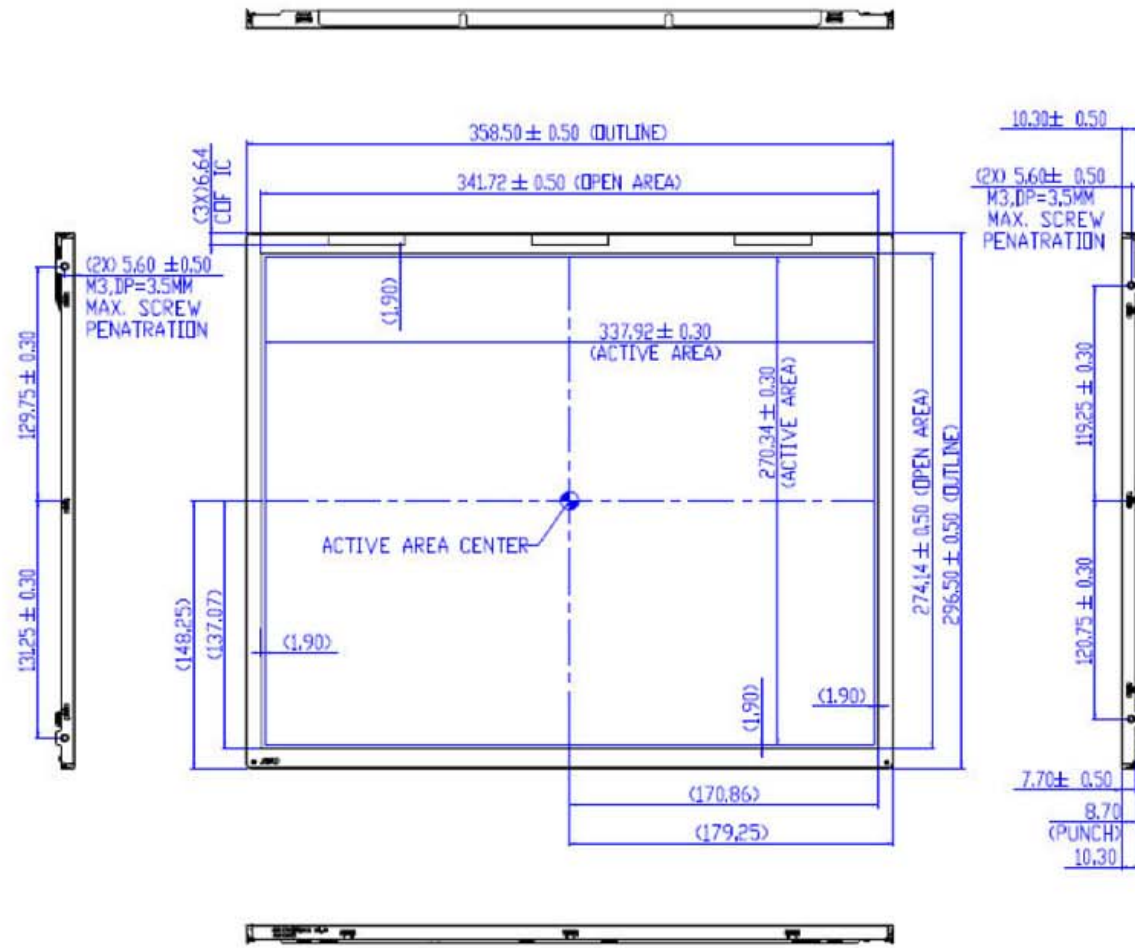


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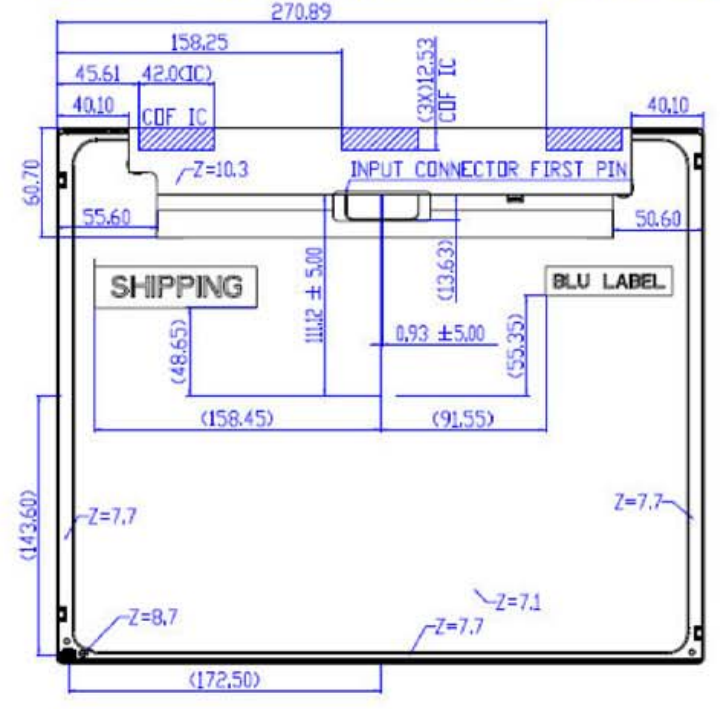
| | | | |
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| 1 | 2 | 3 | 4 |
| 文件題目 | 圖號 | 頁 | 次頁 |
| 發行日 | 舊版日 | 登入號碼 | 機密等級 |

| | | | |
|-----|------|------------------------|-----------------|
| 7 | | 8 樣式 QT3-RD-E-0004-003 | |
| No. | 修訂區域 | 修訂內容 | 作成 修訂日期 |
| | | 新版 | Alan 2013.06.25 |

4. OUTLINE DIMENSIONS



Avoid Touching IC Position When Doing Mechanical Design



- NOTE:
- Unit:mm
 - Without Tolerance ±0.3
 - CN1:MSB240420HD or Compatible
 - CN2:3808K-F05N-02R or Compatible

| | | | | |
|----|---------|--------|-------------|------------------|
| 備考 | 單位:mm | | 投影法: | 比例尺: 1:1 |
| 入庫 | 製圖 Alan | 130625 | 名稱: 17" LCM | 圖號 CH170CLJL-001 |
| | 審查 | | | |
| | 承認 | | | |

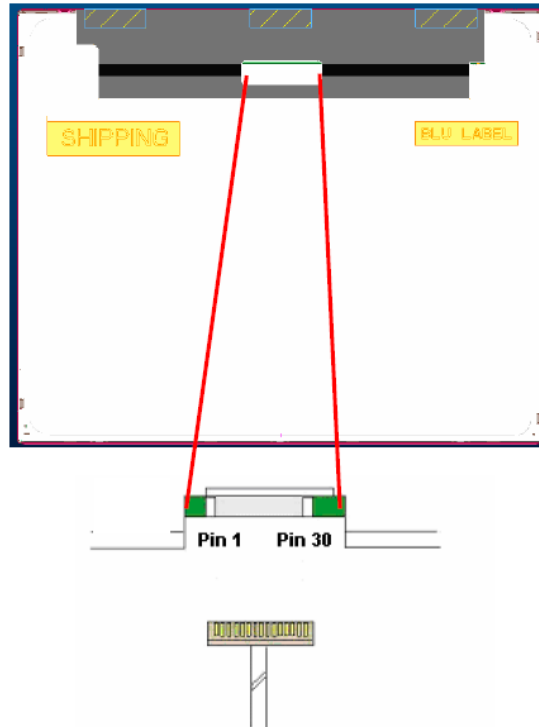
5. INTERFACE PIN CONNECTION

5.1 LCM PANEL DRIVING SECTION

Connector: HKZD52NNUNC/J H37 or Equivalent

| PIN # | SIGNAL NAME | DESCRIPTION |
|-------|-------------|--|
| 1 | RxO0- | Negative LVDS differential data input (Odd data) |
| 2 | RxO0+ | Positive LVDS differential data input (Odd data) |
| 3 | RxO1- | Negative LVDS differential data input (Odd data) |
| 4 | RxO1+ | Positive LVDS differential data input (Odd data) |
| 5 | RxO2- | Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) |
| 6 | RxO2+ | Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) |
| 7 | GND | Power Ground |
| 8 | RxOC- | Negative LVDS differential clock input (Odd clock) |
| 9 | RxOC+ | Positive LVDS differential clock input (Odd clock) |
| 10 | RxO3- | Negative LVDS differential data input (Odd data) |
| 11 | RxO3+ | Positive LVDS differential data input (Odd data) |
| 12 | RxE0- | Negative LVDS differential data input (Even data) |
| 13 | RxE0+ | Positive LVDS differential data input (Even data) |
| 14 | GND | Power Ground |
| 15 | RxE1- | Negative LVDS differential data input (Even data) |
| 16 | RxE1+ | Positive LVDS differential data input (Even data) |
| 17 | GND | Power Ground |
| 18 | RxE2- | Negative LVDS differential data input (Even data) |
| 19 | RxE2+ | Positive LVDS differential data input (Even data) |
| 20 | RxEC- | Negative LVDS differential clock input (Even clock) |
| 21 | RxEC+ | Positive LVDS differential clock input (Even clock) |
| 22 | RxE3- | Negative LVDS differential data input (Even data) |
| 23 | RxE3+ | Positive LVDS differential data input (Even data) |
| 24 | GND | Power Ground |
| 25 | GND | Power Ground (For AUO test Aging+HVS mode) |
| 26 | NC | No contact |
| 27 | GND | Power Ground |
| 28 | VCC | +5.0V Power Supply |
| 29 | VCC | +5.0V Power Supply |
| 30 | VCC | +5.0V Power Supply |

Note1: Start from left side



Note2: Input signals of odd and even clock shall be the same timing.

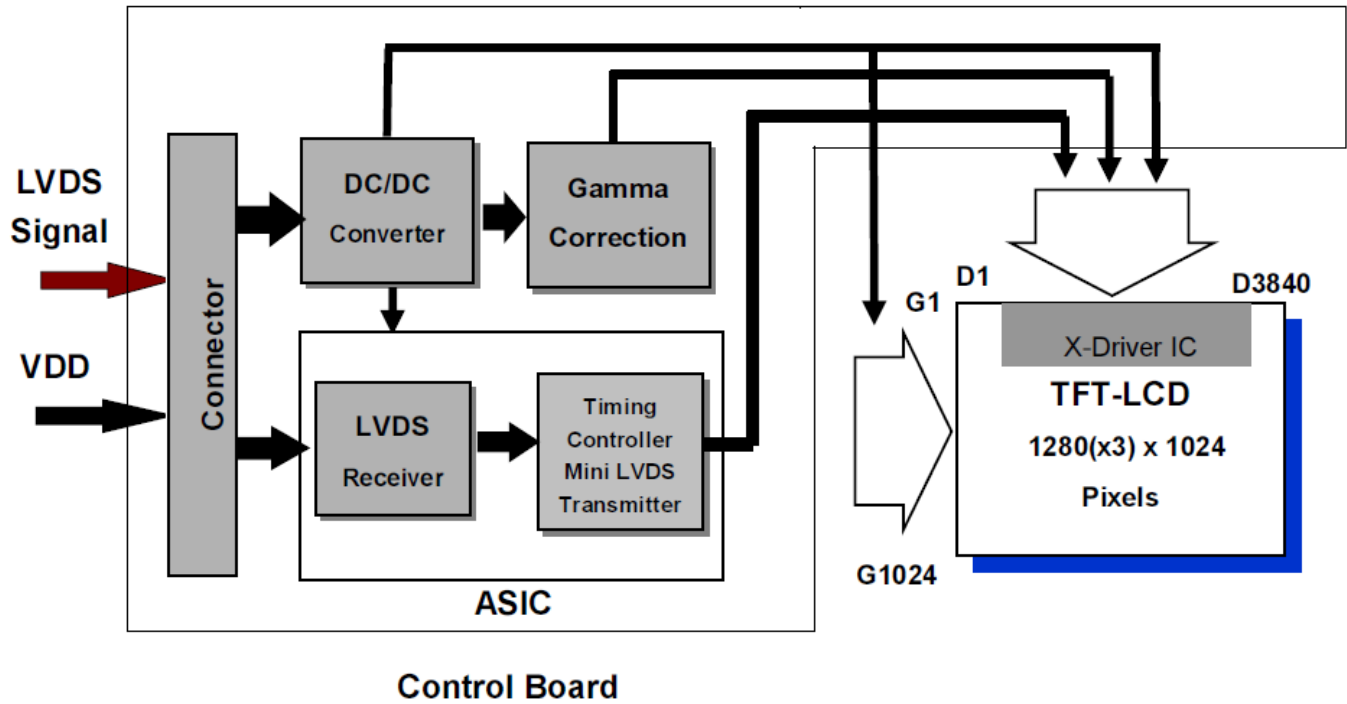
Note3: Please follow PSWG.

5.2 LED INTERFACE CONNECTOR

Connector: CviLux CI0106M1HR0-LF or Equivalent

| PIN NO. | SYMBOL | FUNCTION | REMARK |
|---------|---------|---|--------|
| 1 | VIN | 12V | |
| 2 | VIN | 12V | |
| 3 | Enable | 3V-On / 0V-Off | |
| 4 | Dimming | 0V-Max. brightness / 3V-Min. brightness | |
| 5 | GND | Ground | |
| 6 | GND | Ground | |

6. BLOCK DIAGRAM



7. ABSOLUTE MAXIMUM RATINGS

7.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | MIN. | MAX. | UNIT | REMARK |
|---------------|--------|------|------|------|--------|
| Power Voltage | VDD | -0.3 | 6 | V | |

7.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

| ITEM | OPERATING | | STORAGE | | REMARK |
|-------------------------|-----------|------|---------|------|------------|
| | MIN. | MAX. | MIN. | MAX. | |
| Ambient Temperature(°C) | -10 | 60 | -20 | 70 | Note 1,2,3 |
| Humidity(% RH) | 10 | 90 | 10 | 90 | Note 4 |

Note 1 : The response time will become lower when operated at low temperature.

Note 2 : Background color changes slightly depending on ambient temperature.

Note 3 : Operation $T_a=60^\circ\text{C}$ & $-10^\circ\text{C} \leq 240\text{Hrs}$.

Note 4 : Operation $T_a=50^\circ\text{C}$ & $\text{RH}=80\% \leq 240\text{Hrs}$.

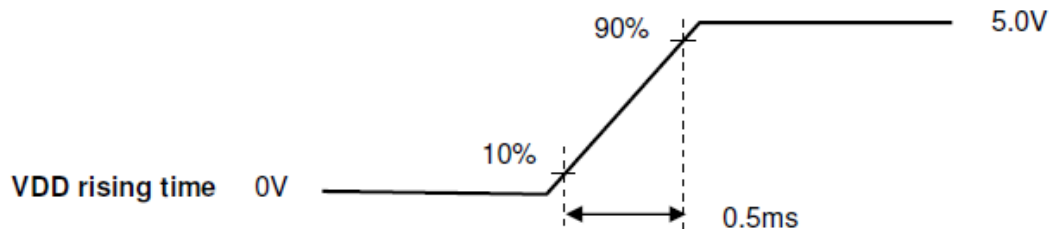
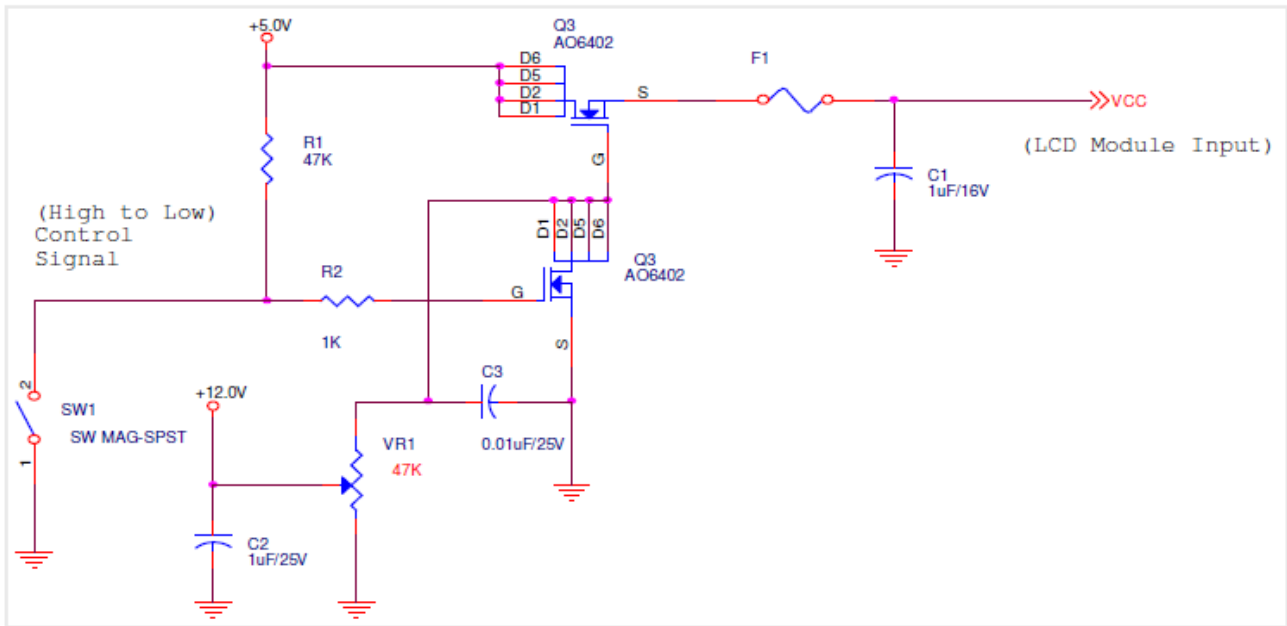
8. ELECTRICAL CHARACTERISTICS

8.1 ELECTRICAL CHARACTERISTICS OF LCD

Ta=25°C

| ITEM | SYMBOL | MIN. | TYP. | MAX. | UNIT | REMARK |
|-----------------------|--------|------|------|------|------|------------------|
| Power Voltage For LCD | VDD | 4.5 | 5.0 | 5.5 | V | - |
| | IDD | - | 600 | 720 | mA | 5V/Black pattern |
| | PDD | - | 3 | - | W | 5V/Black Pattern |
| | Irush | - | - | 3 | A | Note1 |

Note 1: Measure Condition



8.2 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when V_{in} is off

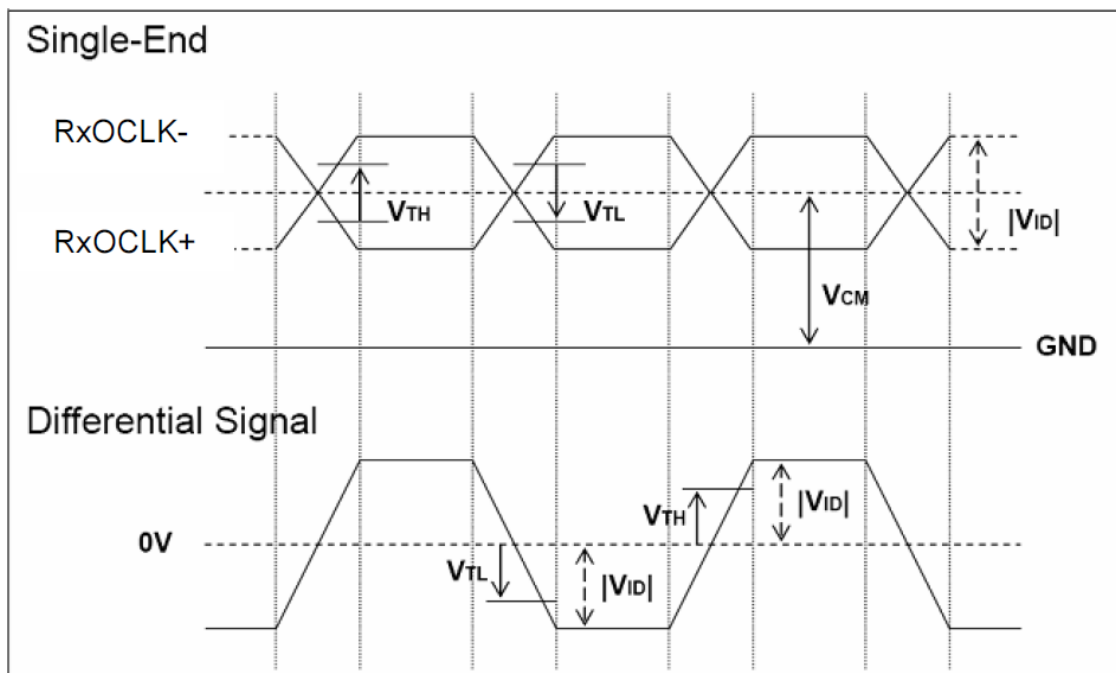
It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Characteristics of each signal are as following:

| Symbol | Description | Min | Typ | Max | Units | Condition |
|------------|--|------|------|------|-------|---------------------------|
| V_{TH} | LVDS Differential Input High Threshold | - | - | +100 | [mV] | $V_{CM} = 1.2V$ |
| V_{TL} | LVDS Differential Input Low Threshold | -100 | - | - | [mV] | $V_{CM} = 1.2V$ |
| $ V_{ID} $ | LVDS Differential Input Voltage | 100 | - | 600 | [mV] | |
| V_{CM} | LVDS Common Mode Voltage | +1.0 | +1.2 | +1.5 | [V] | $V_{TH} - V_{TL} = 200mV$ |

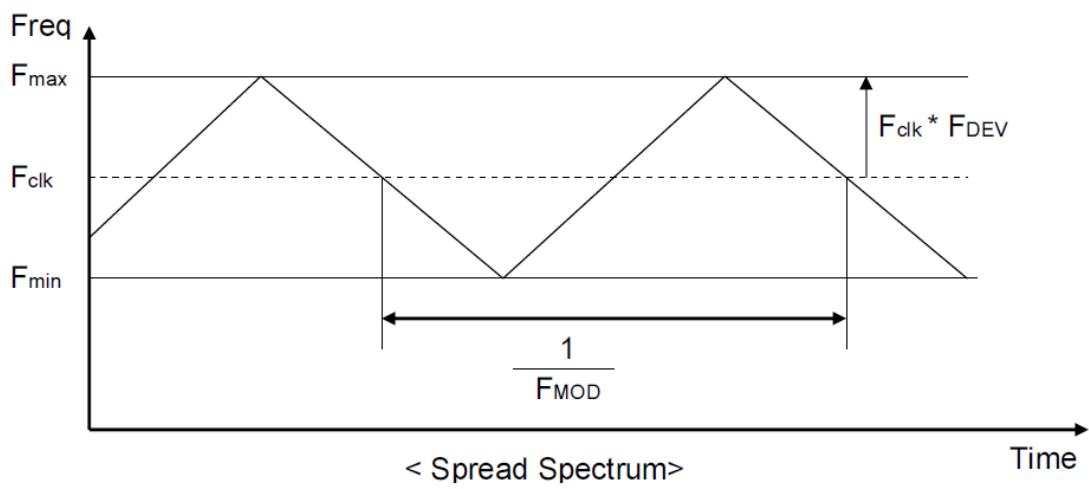
LVDS Signal Waveform:

Use RxOCLK- & RxOCLK+ as example



AC Characteristics:

| Symbol | Description | Min | Max | Unit | Remark |
|-----------|--|-----|---------|------|--------|
| F_{DEV} | Maximum deviation of input clock frequency during Spread Spectrum | - | ± 3 | % | |
| F_{MOD} | Maximum modulation frequency of input clock during Spread Spectrum | - | 200 | KHz | |



Fclk: LVDS Clock Frequency

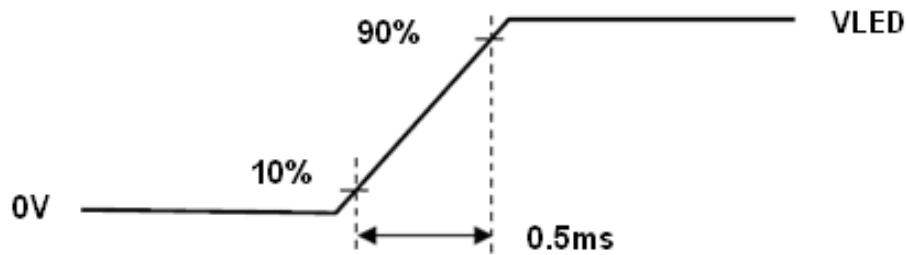
8.2 BACKLIGHT CHARACTERISTICS

Ta=25°C

| ITEM | SYMBOL | MIN. | TYP. | MAX. | UNIT | REMARK |
|-----------------------|--------|--------|------|------|-------|------------------|
| LED Input | VLED | 10.8 | 12 | 13.2 | V | Note 2 |
| LED Power Consumption | PLED | - | - | TBD | W | Note 2 |
| ON/OFF Control | ON/OFF | 0 | - | 3 | V | ON3V;OFF0V |
| Dimming Control | DIM | 0 | - | 3 | V | Max. 0V; Min. 3V |
| LED Life Time | LT | 40,000 | - | - | Hours | Note 1 |

Note 1: The LED life time define as the estimated time to 50% degradation of initial luminous.

Note 2: A higher LED power supply voltage will result in better power efficiency. Keep the VLED between 12V and 13.2V is strongly recommended.



VLED rising time

9.OPTICAL CHARACTERISTICS

Ta=25°C

| ITEM | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | REMARK | |
|----------------|--------|---------------|---|------|------|-------|----------|----------|
| Contrast Ratio | CR | | 600 | 1000 | - | - | Note (1) | |
| Response Time | TR | | - | 3.8 | - | ms | Note (2) | |
| | TF | | - | 1.2 | - | ms | | |
| | TR+TF | | - | 5 | - | ms | | |
| Chromaticity | White | Wx | Viewing Normal Angle $\Theta_x=\Theta_y=0^\circ$ | TBD | TBD | TBD | - | Note (4) |
| | | Wy | | TBD | TBD | TBD | - | |
| | Red | Rx | | TBD | TBD | TBD | - | |
| | | Ry | | TBD | TBD | TBD | - | |
| | Green | Gx | | TBD | TBD | TBD | - | |
| | | Gy | | TBD | TBD | TBD | - | |
| | Blue | Bx | | TBD | TBD | TBD | - | |
| | | By | | TBD | TBD | TBD | - | |
| Viewing Angle | Hor. | Θ_{x+} | Viewing Angle $\Theta_x=\Theta_y=0^\circ$ CR ≥ 10 | 75 | 85 | - | Deg. | Note (3) |
| | | Θ_{x-} | | 75 | 85 | - | | |
| | Ver. | Θ_{y+} | | 75 | 85 | - | | |
| | | Θ_{y-} | | 75 | 85 | - | | |
| Lminance | L | CENTER | 560 | 700 | - | cd/m2 | | |
| Uniformity | | | 65 | 75 | | % | Note (5) | |

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

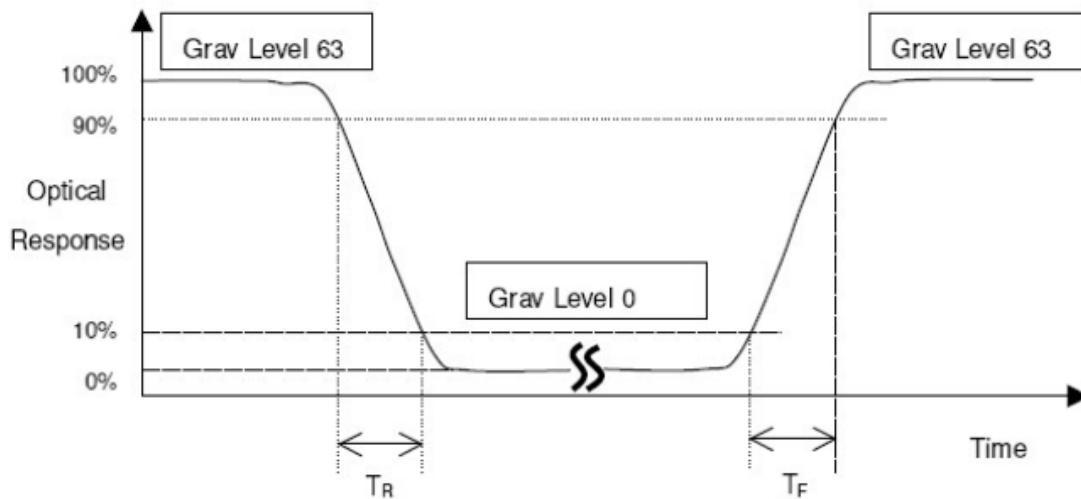
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

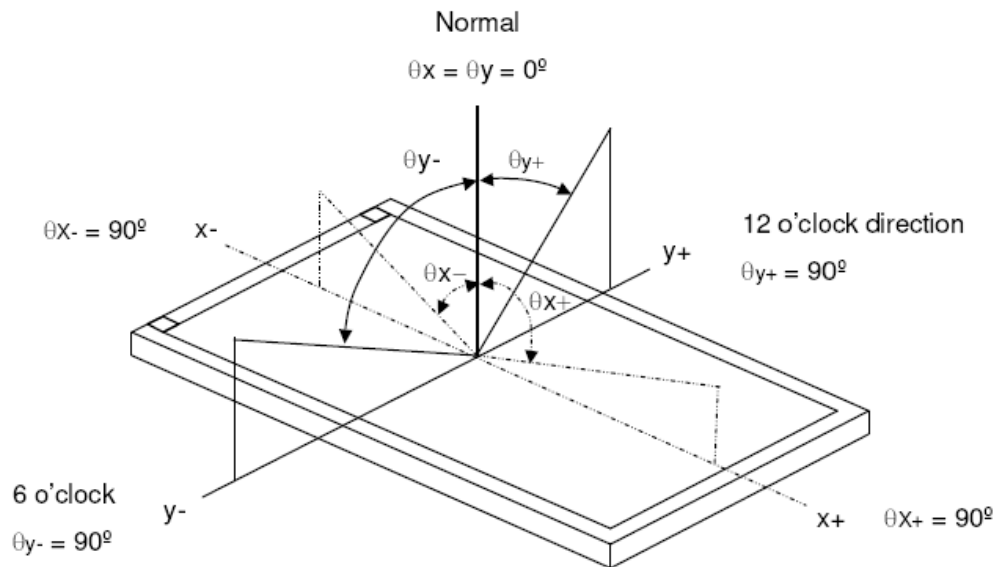
$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time (T_R , T_F):

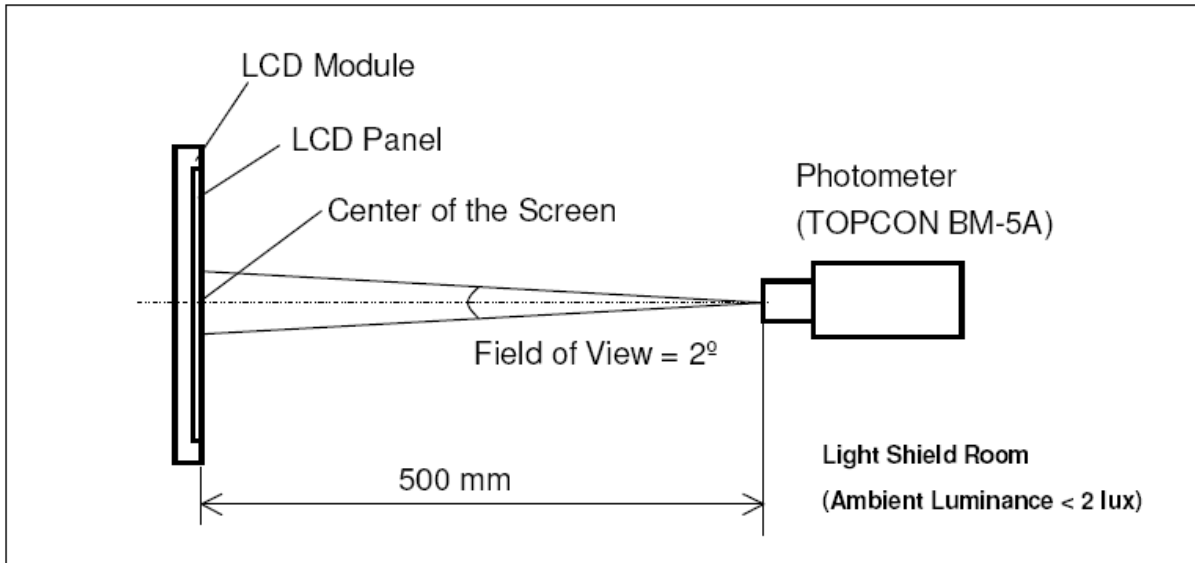


*Note(3) Definition of Viewing Angle

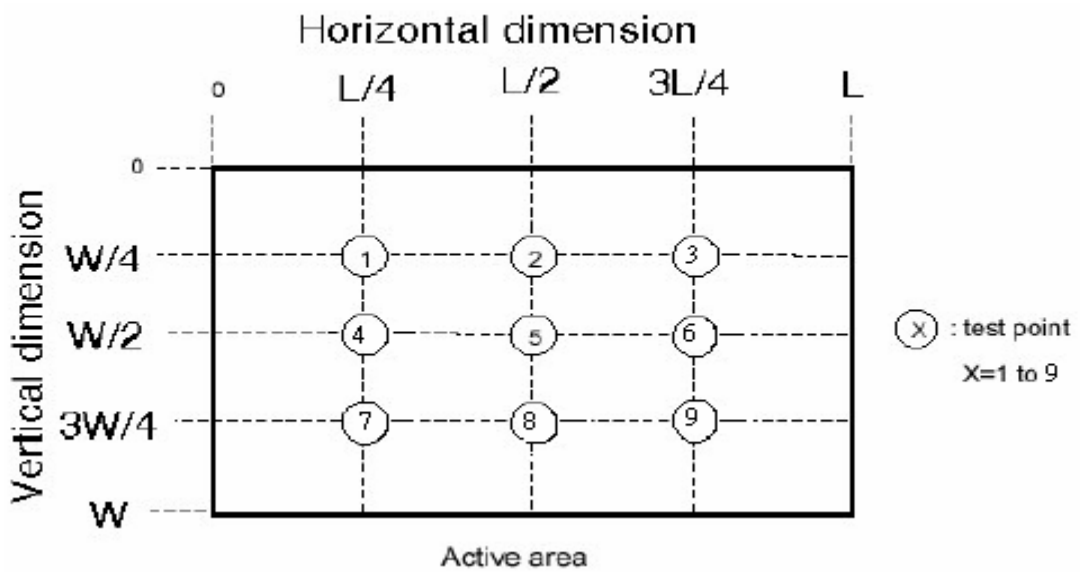


*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



*Note (5)



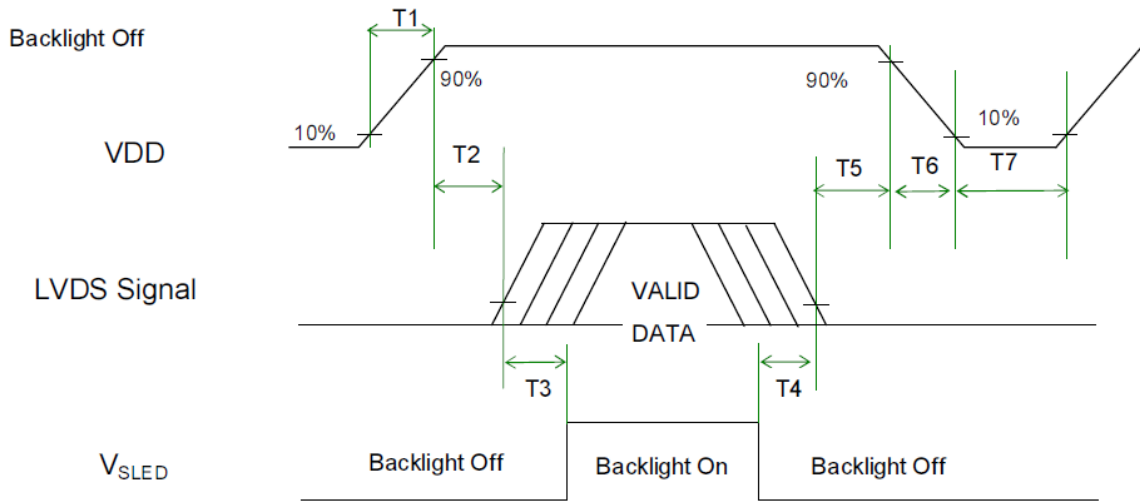
$$\left(1 - \frac{\text{MAX Luminance} - \text{Average Luminance}}{\text{Average Luminance}} \right) \times 100\% > 75\%$$

10. TIMING SPECIFICATIONS

10.1 POWER SIGNAL SEQUENCE

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off. a. Power on sequence:

Power Sequence



Power ON/OFF sequence timing

| Symbol | Value | | | Unit | Remark |
|--------|-------|------|------|------|------------------------------------|
| | Min. | Typ. | Max. | | |
| T1 | 0.5 | - | 10 | [ms] | |
| T2 | 0 | - | 50 | [ms] | |
| T3 | 500 | - | - | [ms] | |
| T4 | 100 | - | - | [ms] | |
| T5 | 0 | | 50 | [ms] | <i>Note 3-5</i> <i>Note 3-6</i> |
| T6 | 0 | - | 150 | [ms] | <i>Note 3-6</i> |
| T7 | 1000 | - | - | [ms] | |

Note: The values of the table are follow PSWG.

10.2 TIMING CHARACTERISTICS

10.2.1. Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

| Symbol | Description | | Min. | Typ. | Max. | Unit | Remark |
|-----------|--------------------|-----------|------|------|------|------|-----------------|
| Tv | Vertical Section | Period | 1036 | 1066 | 1873 | Th | |
| Tdisp (v) | | Active | 1024 | 1024 | 1024 | Th | |
| Tblk (v) | | Blanking | 12 | 42 | 849 | Th | |
| Fv | | Frequency | 50 | 60 | 76 | Hz | |
| Th | Horizontal Section | Period | 730 | 844 | 1320 | Tclk | |
| Tdisp (h) | | Active | 640 | 640 | 640 | Tclk | |
| Tblk (h) | | Blanking | 90 | 204 | 680 | Tclk | |
| Fh | | Frequency | 37.8 | 54 | 68.4 | KHz | Note 3-3 |
| Tclk | LVDS Clock | Period | 50 | 60 | 76 | ns | 1/Fclk |
| Fclk | | Frequency | 51.8 | 64 | 93.7 | MHz | Note 3-4 |

Note: The equation is listed as following. Please don't exceed the above recommended value.

$$Fh (\text{Min.}) = Fclk (\text{Min.}) / Th (\text{Min.});$$

$$Fh (\text{Typ.}) = Fclk (\text{Typ.}) / Th (\text{Typ.});$$

$$Fh (\text{Max.}) = Fclk (\text{Max.}) / Th (\text{Min.});$$

Note: The equation is listed as following. Please don't exceed the above recommended value.

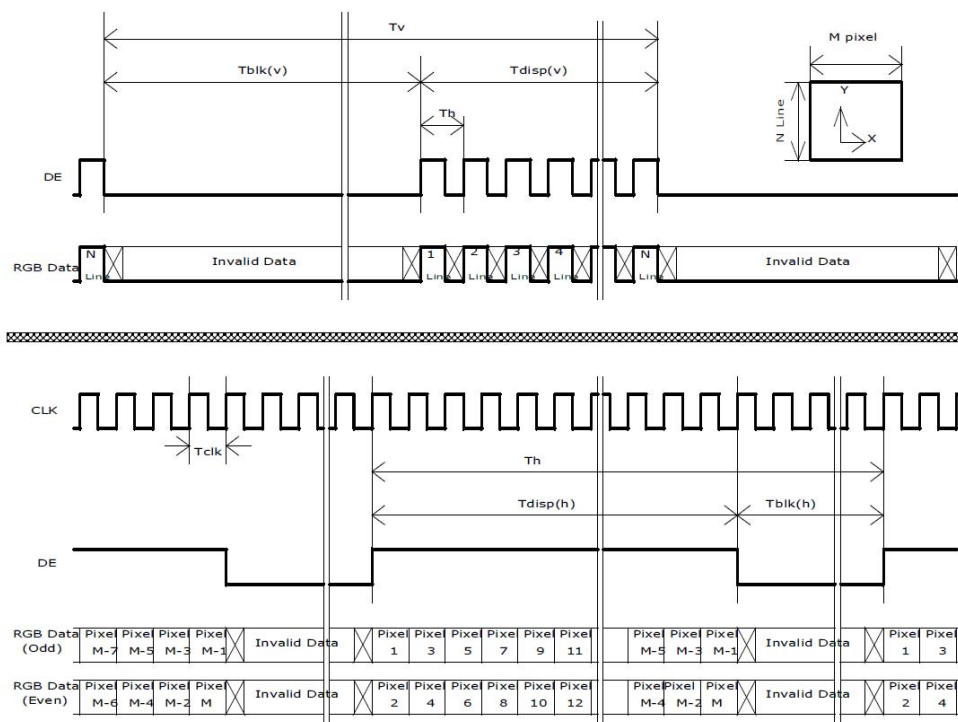
$$Fclk (\text{Min.}) = Fv (\text{Min.}) \times Th (\text{Min.}) \times Tv (\text{Min.});$$

$$Fclk (\text{Typ.}) = Fv (\text{Typ.}) \times Th (\text{Typ.}) \times Tv (\text{Typ.});$$

$$Fclk (\text{Max.}) = Fv (\text{Max.}) \times Th (\text{Typ.}) \times Tv (\text{Typ.});$$

10.2.2. Timing Diagram of Interface Signal

Timing Characteristics



11. RELIABILITY TEST

Ta = 25°C

Environment test conditions are listed as following table.

| Items | Required Condition | Note |
|----------------------------------|---|------|
| Temperature Humidity Bias (THB) | Ta= 50°C, 80%RH, 300hours | |
| High Temperature Operation (HTO) | Ta= 60°C, 50%RH, 300hours | 3 |
| Low Temperature Operation (LTO) | Ta= -10°C, 300hours | |
| High Temperature Storage (HTS) | Ta= 70°C, 300hours | |
| Low Temperature Storage (LTS) | Ta= -20°C, 300hours | |
| Drop Test | Height: 60 cm, package test | |
| Thermal Shock Test (TST) | -20°C/30min, 60°C/30min, 100 cycles | 1 |
| On/Off Test | On/10sec, Off/10sec, 30,000 cycles | |
| ESD (ElectroStatic Discharge) | Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point. | 2 |
| | Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point. | 2 |

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: The test items are tested by open frame type chassis.

12. PRECAUTIONS FOR USE

12.1 Safety

- (1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
- (2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
- (3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

12.2 Storage Conditions

- (1) Store the panel or module in a dark place where the temperature is $23\pm 5^{\circ}\text{C}$ and the humidity is below $50\pm 20\%\text{RH}$.
- (2) Store in anti-static electricity container.
- (3) Store in clean environment, free from dust, active gas, and solvent.
- (4) Do not place the module near organics solvents or corrosive gases.
- (5) Do not crush, shake, or jolt the module.

12.3 Handling Precautions

- (1) Avoid static electricity which can damage the CMOS LSI.
- (2) The polarizing plate of the display is very fragile. So, please handle it very carefully.
- (3) Do not give external shock.
- (4) Do not apply excessive force on the surface.
- (5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the Surface of plate.
- (6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
- (7) Do not operate it above the absolute maximum rating.
- (8) Do not remove the panel or frame from the module.
- (9) When the module is assembled, it should be attached to the system firmly, Be careful not to twist and bend the module.
- (10) Wipe off water droplets or oil immediately . If you leave the droplets for a long time, staining and discoloration may occur.
- (11) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

12.4 Warranty

(1) Acceptance inspection period

The period is within one month after the arrival of contracted commodity at the buyer's factory site.

(2) Applicable warrant period

The period is within 12 months since the date of shipping out under normal using and storage conditions.